Comparative Analysis of Different Logics of Demultiplexer

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***Abstract*: Low power and high speed digital circuits are basic needs for any of digital circuit; De-multiplexer is a basic circuit for any digital circuit. In this paper de-multiplexer has been designed using CMOS, transmission gate pseudo nmos logic. The performance of designs has been compared in terms of power consumption, delay and transistor counts. The proposed design demonstrates the superiority in terms of power dissipation, delay and transistor counts, compared with existing 1:4 de-multiplexer and comparative analysis on 90nm and 45nm technology. The schematic of developed de-multiplexer has been designed and simulated using Tanner EDA tool.**

***Index Terms:* De-multiplexer, CMOS, Transmission gate, pseudo NMOS gate, Power dissipation, delay.**

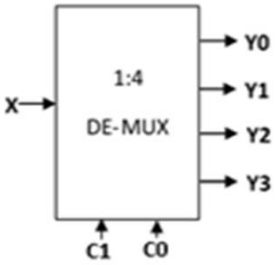
INTRODUCTION

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. The reduction of the power consumption by any VLSI circuit basically depends on the some parameters viz. reducing the number of transistor, reducing the size of the transistor, input re-ordering, reducing the capacitance etc. Transistor size optimization is one method to reduce the power dissipation of CMOS VLSI circuits. It is generally believed that low power designs need to have minimum transistor size. Most of the low-power design techniques are effective only for specific types of circuits and applications. Delay and power dissipation of a circuit have also emerged as major concerns of designers and depend on the number of transistors used in the circuit. So here our aim is to reduce the delay and power dissipation. In this paper the author is applying technique like reducing the number of transistors, switching off some part of circuit during different input conditions and using different elements in the implementation of the circuit to reduce the overall power consumption.

This paper analyzes 1:4 De-multiplexer using complementary CMOS, transmission gate and pseudo logic styles. These implementations are compared based on the basis of transistor count, power dissipation, and delay analysis.

De-multiplexer (or de-mux) is a device that selects one of several analog or digital input signals and forwards the selected single input into a multiple line. A de-multiplexer of single inputs has n select lines, which are used to select which input line to send to the 2n output line. De-multiplexers perform the opposite function of multiplexers. They transfer a small number of Information units (usually one unit) over a larger number of channels under the control of Selection signals.

In the circuit C1 and C0 are selection bits and X is the data bit. Depending upon the states of the selection bits, the data X is transferred to one of the four output connections. The routing of data bit on different output connections based on states of the selection bits is shown in Fig. 1.



I/P	SELECT INPUTS		OUTPUT			
	C1	C0	Y0	Y1	Y2	Y3
X	0	0	X	0	0	0
X	0	1	0	X	0	0
X	1	0	0	0	X	0
X	1	1	0	0	0	X

Fig. 1 De-multiplexer and its truth table

DIFFERENT LOGIC STYLES

A logic style is the way how a logic function is implemented using a set of transistors. Various characteristics like speed, size, power dissipation and wiring complexity depend on a logic style and may vary considerably from one logic style to another and thus choice of proper logic style is very important for circuit performance. This paper shows three logic styles like Complementary MOS, Transmission gate and Pseudo nmos logic.

1) **COMPLEMENTARY MOS LOGIC STYLE:** Conventional de-multiplexer circuits are made using AND gates and inverters (NOT gates). In order to design a 1x4 de-multiplexer circuit, two inverter and four numbers of three input AND gates are required. A single AND gate with three inputs requires eight transistors to be used for implementation. In this way the number of transistors used for implementing total four numbers of three input AND gates becomes thirty two. In addition to this, the number of transistors required to implement two inverters are four. In all the implementation of 1x4 multiplexer using the conventional method requires thirty six transistors. The implementation of conventional de-multiplexer circuit using AND gates and inverters are shown in Fig. 2.

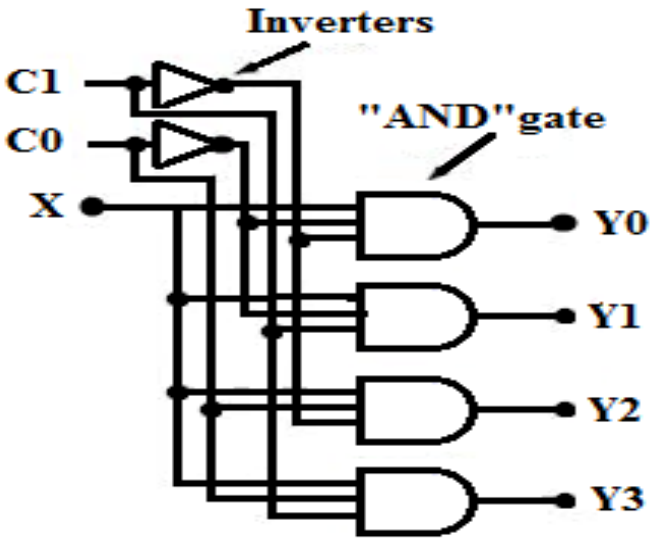


Fig. 2 Conventional CMOS 1:4 De-multiplexer

2) **TRANSMISSION GATE (TG) LOGIC STYLE:** The most widely used solution to deal with the voltage drops induced by pass transistors is the use of transmission gates. The primary limitation of NMOS or PMOS only pass gate is the threshold voltage drop (NMOS pass device pass a strong 0 while passing a weak 1 and PMOS pass devices pass a strong 1 while passing a weak 0). The ideal approach is to use the NMOS device to pull-down and the PMOS device to pull-up. The transmission gate combines the best of both devices placing a NMOS device in parallel with a PMOS device.

The control signals to the transmission gate (C and C-bar) are complementary. The transmission gate acts as a bidirectional switch controlled by the gate signal C. When C= 1, both MOSFETs are on, allowing the signal to pass through the gate. On the other hand, C = 0 places both transistors in cutoff, creating an open circuit between nodes A and B. Schematic and circuit symbol of Transmission gate in Fig. 3.

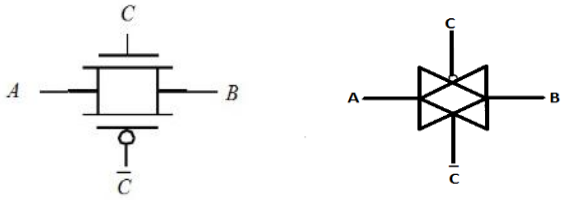


Fig. 3 Schematic and circuit symbol of Transmission gate

The new design consists of total six numbers of transmission gates with two inverters. The implementation of 1:4 de-multiplexer using the transmission gate contains 16 numbers of transistors. The circuit arrangement of the new design is shown in Fig. 4. In De-multiplexer circuit C1 and C0 are selection bits and X is the data bit. Depending upon the states of the selection bits, the data X is transferred to one of the four output connections. The routing of data bit on different output connections based on states of the selection bits.

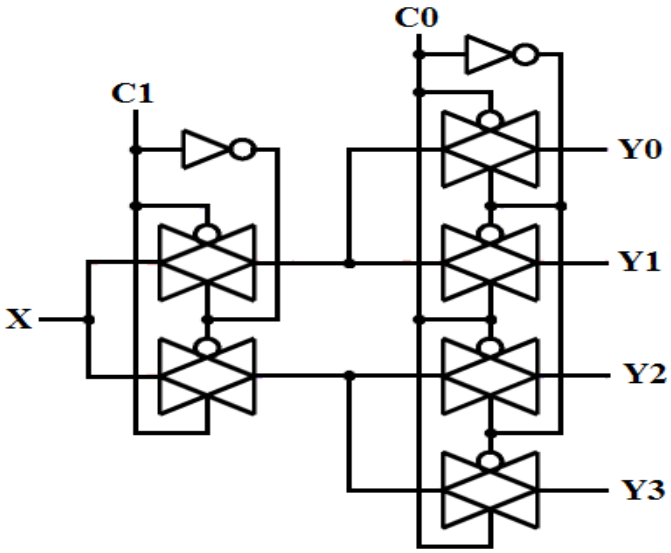


Fig. 4 1:4 De-multiplexer circuit using Transmission gate

3) **PSEUDO N-MOS LOGIC STYLE:** Pseudo NMOS logic is one type of alternate gate circuit that is used as a supplement for the complementary MOS logic circuits. In the pseudo-nMOS logic, the pull up network (PUN) is realized by a single PMOS transistor. The gate terminal of the PMOS transistor is connected to the ground. It remains permanently in the ON state. Depending on the input combinations, output goes low through the PDN.

There are devices in the PDN and the grounded PMOS load device. This result in reduced noise margins propagation delay, and power dissipation. The advantage of a pseudo N-MOS gate is the reduced no. of transistor (N+1 versus 2N for completely CMOS). When the area is most important however its reduced transistor count compared with complementary CMOS.

The inverter that uses a p-device pull-up or load that has its gate permanently ground. An n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is nmos technology and is thus called 'Pseudo-NMOS'. The circuit is used in a variety of CMOS logic circuits.

The pseudo-NMOS inverter contains two interconnected MOSFET transistors: one NMOS transistor (QN) which works as driver and one PMOS-transistor (QP) which works as an active load. Except for the load device, the pseudo-nMOS gate circuit is identical to the pull down network (PDN) of the complementary CMOS gate. The pseudo-NMOS inverter is shown in Fig. 5.

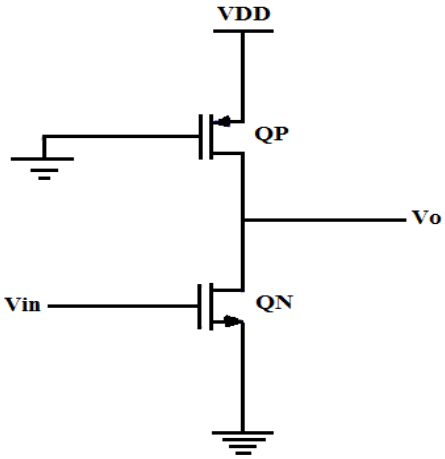


Fig. 5 Pseudo-NMOS inverter

SIMULATION

In this paper different logic styles CMOS, transmission gate and pseudo logic was used to design 1:4 de-multiplexer. These de-multiplexers were designed on S-edit of Tanner tool on 45nm technology and simulated on T-edit with 0.6 to 1v power supply. Figures shows schematics of de-multiplexers designed using three logic styles.

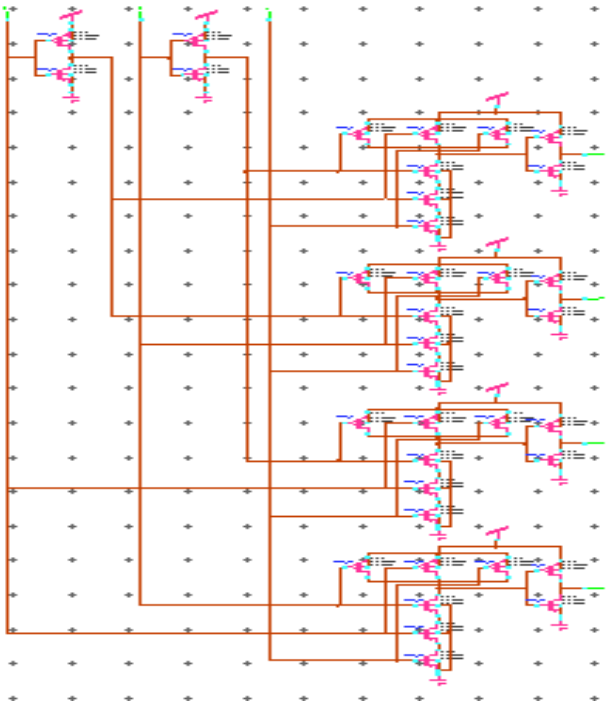


Fig.5.1 Schematic of CMOS 1:4 De-multiplexer on tanner tool
And their simulation result is as shown in figure

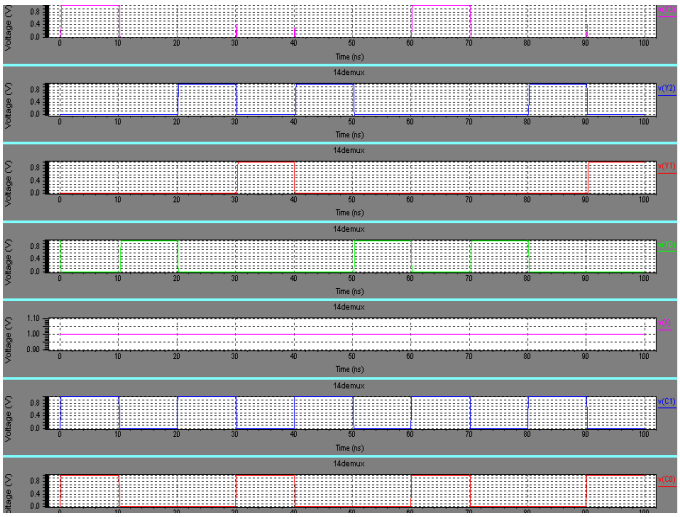


Fig.5.2 Simulation result of CMOS 1:4 De-multiplexer

And the Schematic of Transmission Gate 1:4 De-mux is given as

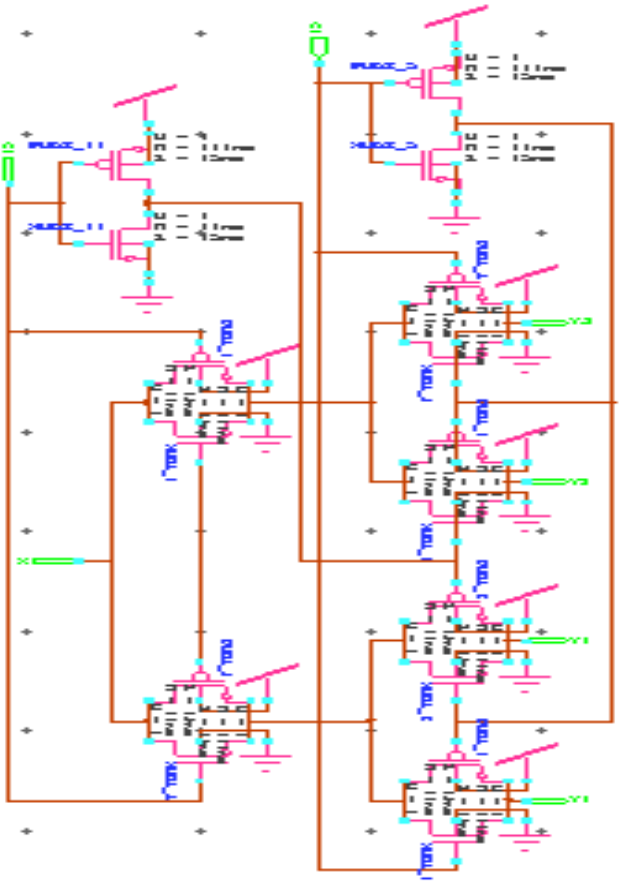


Fig.5.3 Schematic of TG de-multiplexer on tanner tool

And their Simulation result is given as

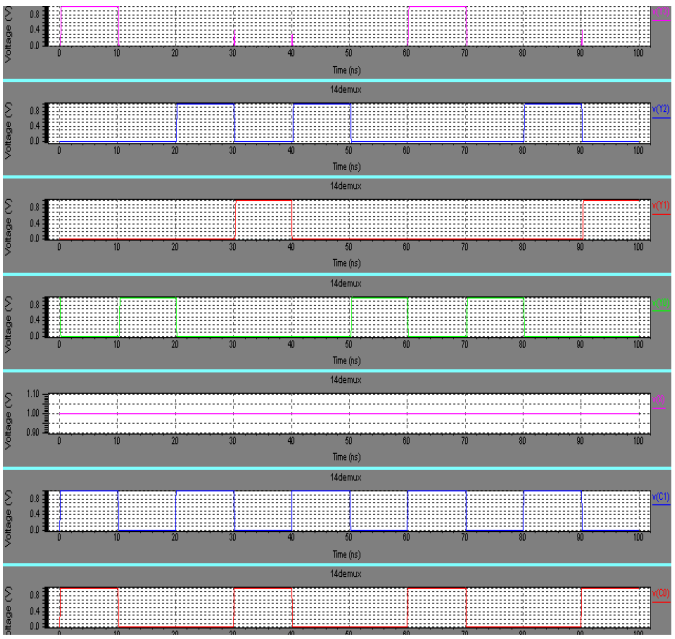


Fig.5.4 Simulation result of Transmission gate De-mux

And Schematic of Pseudo logic 2:1 De-mux is

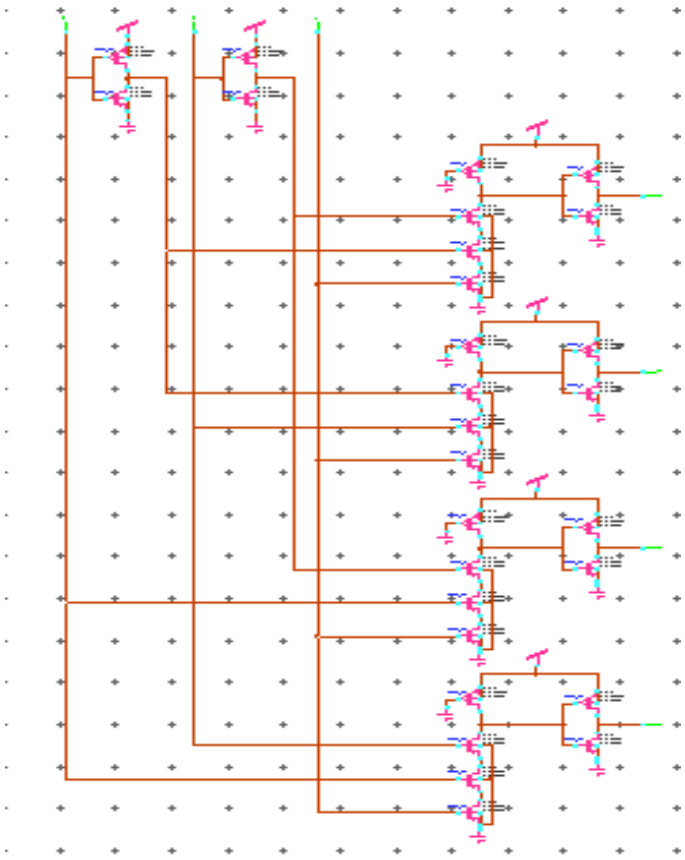


Fig.5.5 Schematic of Pseudo logic multiplexer on tanner tool

And their simulation result is as shown in figure

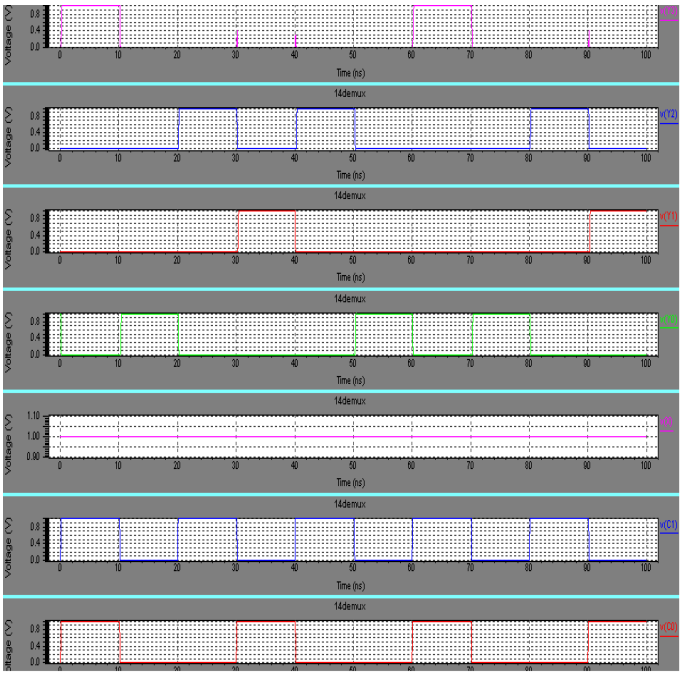


Fig.5.6 Simulation result of Pseudo logic based 1:4 De-mux

EXPERIMENTAL RESULTS

Different parameters of conventional de-multiplexer circuit and other made using transmission gate are compared in the table.

S. No.	Properties		1:4 DE-MUX using CMOS gate	1:4 DE-MUX using transmission gate	1:4 DE-MUX using Pseudo gate
1.	No. of transistors		36	16	28
2.	Power consumption	0.6V	4.151888e-007watts	7.9949165e-008watts	5.232407e-006watts
		0.8V	7.274191e-007watts	1.342190e-007watts	1.670889e-005watts
		1V	1.201473e-006watts	2.343169e-007watts	3.255591e-005watts
3.	Delay		1.0027e+000	1.0214e+000	1.7638e-002

From the analysis of both the designs of the de-multiplexer circuits it is evident that the new designed de-multiplexer with transmission gates consumes less power than the conventional de-multiplexer.

CONCLUSION

From the work carried out in this paper for implementation of 1:4 Demultiplexer, we conclude that proposed design of 1:4 de-multiplexer circuit design using different logic styles that shows improved performance than the existing 1:4 de-multiplexer circuit. The above result analysis it is concluded that power dissipation in the proposed circuit is approximately 73.67% than static (conventional design) circuit and 20.38% less delay as compare to static circuit like conventional de-multiplexer designed with gates. The de-multiplexer can operate well up to 1.25 Gb/s. Circuit has been realized using 45nm technology. Proposed design proved to be an attractive alternative to CMOS Based 1:4 DE-MUX designs with respect to area, performance, power consumption and delay analysis. Among all three transistor logic styles considered Transmission Gate Based 1:4 DE-MUX is having few transistor counts.

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