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Ping-Pong Auto-Zero Architecture For High-Accuracy Operational Amplifier Design

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Abstract: Many electronic systems rely on processing small signal inputs, making low offset and minimal offset drift over time and temperature essential. Applications in instrumentation, automotive, and industrial sectors demand high-precision amplifiers that are both cost-effective and simple to implement. Among various solutions, auto-zero amplifiers offer the lowest offset and drift performance. This thesis presents the design of a precision operational amplifier using a ping-pong auto-zero architecture. The proposed design ensures continuous output while achieving extremely low offset and drift over a wide temperature range, making it suitable for harsh environments. Simulated results demonstrate an input-referred offset voltage of less than 15 µV and an offset drift of 3.5 µV/°C. The design, implemented using Cadence 0.18 µm CMOS technology, consumes 4.2 mW of power.

Index Terms **- Precision Operational Amplifier, Auto-Zero Amplifier, Ping-Pong Architecture, High Precision Analog Design.**

I. INTRODUCTION

Operational amplifiers (op-amps) are indispensable components in analog and mixed-signal systems, serving as the backbone of applications ranging from precision instrumentation to data conversion. At the heart of every op-amp lies the differential amplifier, a circuit designed to amplify the difference between two input signals while rejecting common-mode noise. Despite its theoretical elegance, real-world implementations of differential amplifiers are plagued by input offset voltage—a small but critical DC voltage mismatch between the input terminals. This offset, often caused by manufacturing variations in transistor pairs, temperature drift, and aging, introduces errors that degrade system accuracy, particularly in high-gain or low-noise applications such as biomedical sensors and analog-to-digital converters (ADCs).

Traditional methods to mitigate offset, such as chopper stabilization and auto-zeroing, have been widely adopted but suffer from significant limitations. Chopper amplifiers, while effective at suppressing low-frequency noise and offset, impose strict bandwidth restrictions due to their reliance on signal modulation. Auto-zero techniques, on the other hand, sample and cancel offset during dedicated calibration phases but disrupt continuous signal processing, rendering them unsuitable for real-time applications. These trade-offs highlight the need for an architecture that combines the precision of offset cancellation with uninterrupted operation.

This thesis addresses these challenges through the design, analysis, and validation of a Ping-Pong auto-zero architecture, an innovative approach that leverages dual auto-zero amplifiers operating in alternating phases. By ensuring that one amplifier processes the input signal while the other calibrates, the architecture achieves continuous, offset-free amplification—a critical advancement for modern analog systems. The work builds on foundational studies of differential amplifier design and offset cancellation techniques while introducing novel solutions to mitigate charge injection, clock feedthrough, and transient glitches.

II. LITERATURE REVIEW

Operational amplifiers (op-amps) are fundamental to analog design, performing tasks like amplification, filtering, and signal conditioning. A core component, the differential amplifier, enhances voltage differences while rejecting common-mode signals, with its effectiveness measured by the common-mode rejection ratio (CMRR) (Gray et al., 2009). Practical op-amps, however, suffer from input offset voltage caused by transistor mismatches, temperature drift, and aging (Allen & Holberg, 2012). This issue is critical for precision applications, leading to the development of techniques such as chopper stabilization and auto-zeroing.

Research on differential amplifiers shows that mismatches in the input transistor pair degrade CMRR and introduce offset (Huijsing, 2001), while finite output impedance and process variations limit practical gains, often requiring compensation in multi-stage designs (Razavi, 2001). Offset voltage and drift have been linked primarily to 1/f noise and temperature effects, with BJT op-amps achieving lower offsets compared to CMOS counterparts, though CMOS remains attractive for its scalability and efficiency (Enz & Temes, 1996; Burns & Roberts, 2001). Chopper stabilization techniques, introduced by Enz et al. (1995), modulate the input to high frequencies, effectively minimizing low-frequency noise and offset but limiting bandwidth to below 10 kHz (Makinwa et al., 2010). Auto-zeroing, as explained by Burt & Zhang (2007), samples and cancels the offset during specific phases, although switching introduces transient errors, which Pertijs et al. (2005) mitigated through improved circuit techniques. To maintain continuous output, Ping-Pong architectures were developed, alternating between two auto-zeroed amplifiers. This approach achieved low offsets below 5 µV and higher bandwidths, though it introduced challenges such as increased power consumption and clock feedthrough (Wu et al., 2012; Harpe et al., 2018; Souri et al., 2019).

III. PROPOSED SYSTEM

The term ping pong denotes a reciprocal or alternating operation. This architecture comprises two identical amplifiers, a switch, a sample-and-hold circuit, and a switch driver. The necessity for such a configuration arises from the inherent limitation of auto-zero amplifiers, which are unable to generate a continuous output on their own. Auto-zero amplifiers function in two distinct phases: amplification and sampling. Consequently, they cannot maintain continuous signal processing. The ping pong architecture addresses this limitation by utilizing two identical auto-zero amplifiers, such that at any given time, one amplifier is actively processing the input signal while the other performs offset cancellation. This arrangement ensures both continuous signal amplification and continuous offset correction, ultimately yielding a continuous, offset-free output.

The ping pong auto zero block diagram is shown below:

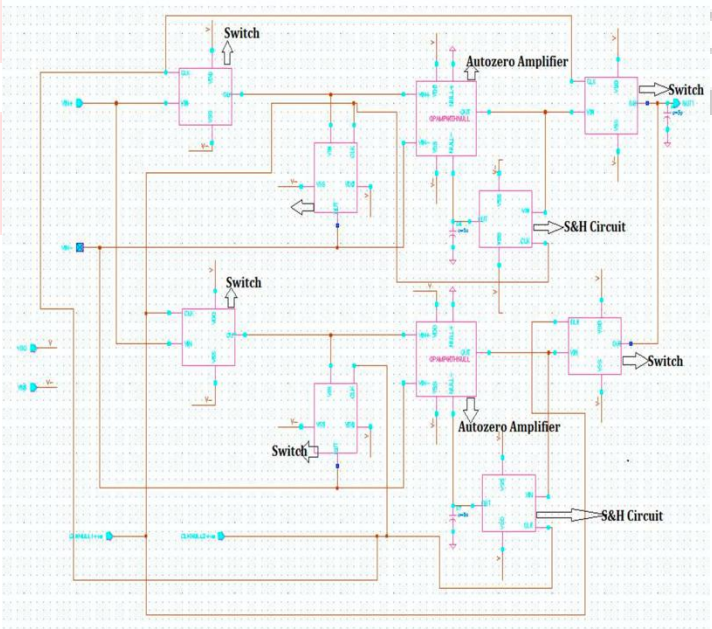

Fig 1: Block diagram of ping pong auto zero amplifier

Components of Ping-Pong Architecture

1. Operational Amplifier with Auto-Zeroing

The classical two-stage operational amplifier is modified by introducing an auxiliary input pair to enable auto-zero functionality. In the ping-pong architecture, two identical auto-zero amplifiers are employed. The gain of the original amplifier (A_v) is equally distributed between the main and auxiliary input paths, resulting in each path having a gain of $A_v/2$. Consequently, the auto-zero amplifier exhibits half the gain of a conventional operational amplifier, while ensuring equal gains for both input pairs.

2. Sample and Hold Circuit

The sample-and-hold (S/H) circuit (shown in Fig. 2) is critical for achieving high accuracy in the design. It samples the input offset voltage during the sampling phase and holds it during the amplification phase, thereby enabling offset-free amplification of the input signal.

A basic implementation using a single NMOS transistor and a capacitor suffers from charge injection and clock feedthrough effects, leading to output inaccuracies.

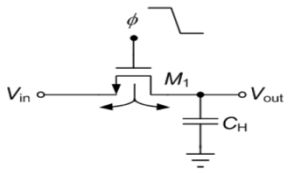

Fig 2: Sample and hold circuit

The **charge injection effect** occurs when charge stored in the channel during the ON phase of the NMOS is transferred to the holding capacitor upon switch-off. The injected charge (Q_{st}) and the resulting residual voltage (ΔV) across the holding capacitor (C_H) are expressed as:

$$Q_{st} = WLC_{ox}(V_{DD} - V_{IN} - V_{th})$$

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{IN} - V_{th})}{C_H}$$

Additionally, the clock feedthrough effect introduces error during the clock's high-to-low transition due to gate-drain and gate-source overlap capacitances, described by:

$$\Delta V = \frac{V_{clk}C_{gd}}{C_{gd} + C_H}$$

To minimize these errors, two techniques are incorporated:

A. Complementary Switching: Both NMOS and PMOS switches are used (Fig. 3) to partially cancel the injected charges due to their opposite polarities. However, complete cancellation is limited by mismatch in gate-drain capacitances.

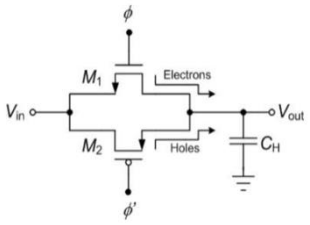

Fig 3: Sample and hold circuit

B. Dummy Switches: As depicted in Fig. 4, dummy switches provide a low impedance path to divert injected charges during switching, further improving accuracy.

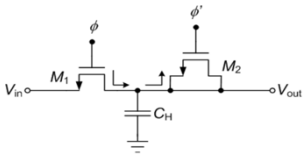

Fig 4: Sample and hold circuit

For robust operation, the clock phases (Φ) and (Φ') must transition without delay. In this design, the selected parameters are $C_H = 5\,\mu F$, $(W/L)_1 = 10$, $(W/L)_2 = 4$ and $(W/L)_{3,4} = 0.5$.

3. Switch and Switch Driver

The switch driver, illustrated in Fig. 5, is essential to ensure synchronized switching of the transistors (M1, M2, M3, and M4) within the S/H circuit. A simple inverter is insufficient due to potential clock skew issues. Instead, a dedicated clock driver generates two overlapping clock signals with minimal skew, enabling simultaneous ON/OFF transitions as required.

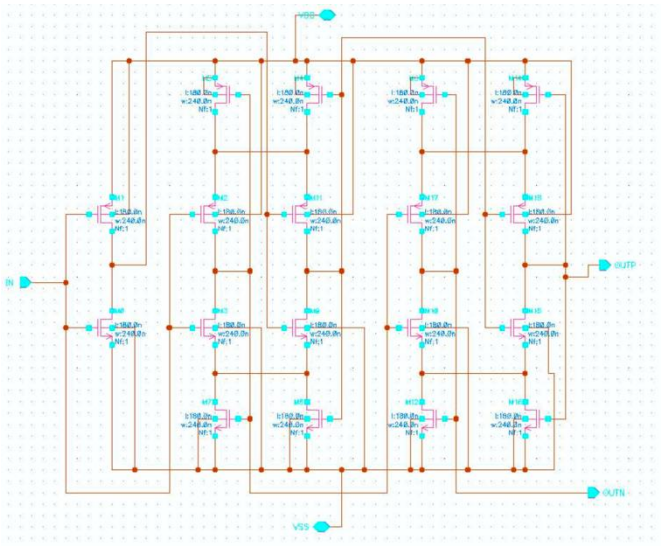

Fig 5: Switch Driver Schematic

CMOS transmission gates, consisting of parallel NMOS and PMOS transistors, are utilized as the switches. In this project, the NMOS is designed with $(W/L) = 10$ and the PMOS with $(W/L) = 4$, ensuring low ON-resistance and reliable switching performance.

IV. RESULTS

1. Offset of basic and Ping-Pong amplifier comparison

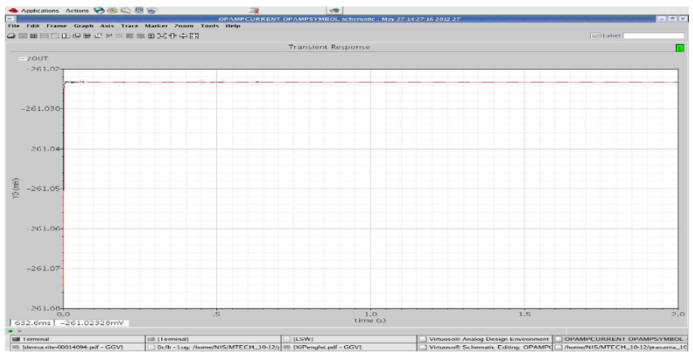

Fig 6: Output offset voltage of basic opamp

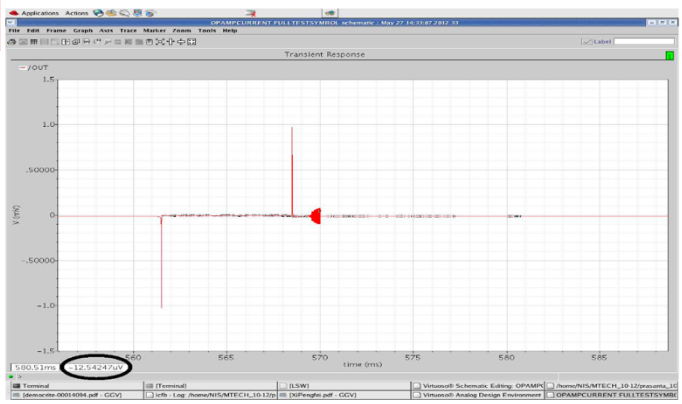

Fig 7: Output offset voltage of Ping-Pong amplifier

2. Offset cancellation of ping pong amplifier

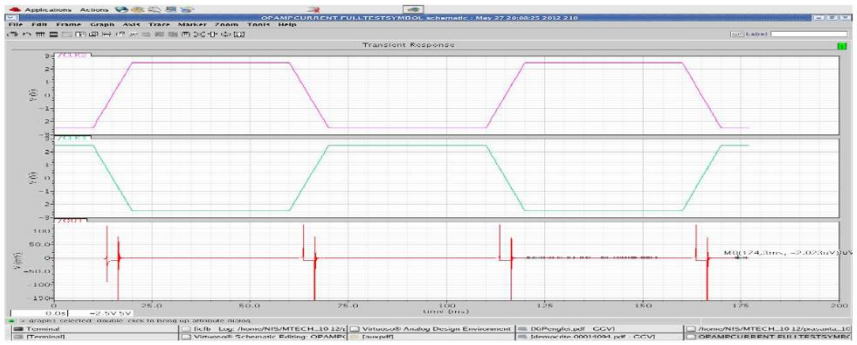

Fig 8: Offset cancellation of ping pong amplifier

3. Other parameters of Ping-Pong amplifier

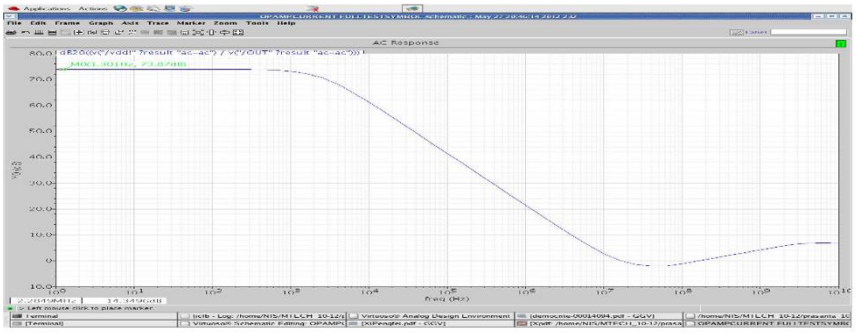

Fig 9: Offset cancellation of ping pong amplifier

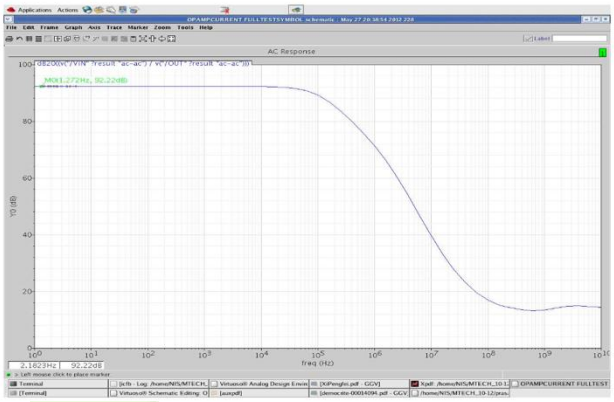

Fig 10: CMRR of ping pong amplifier

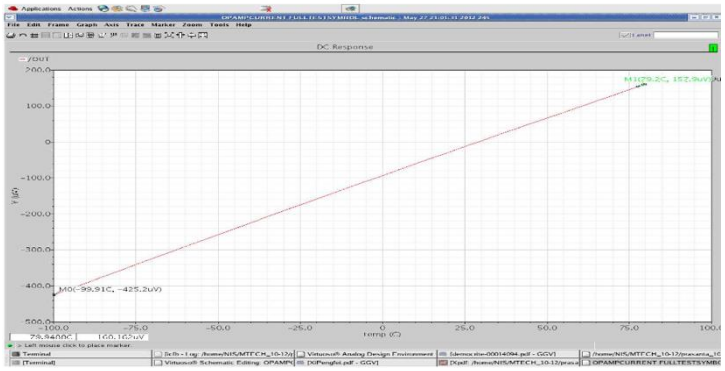

Fig 11: Offset vs. temperature drift of ping pong amplifier

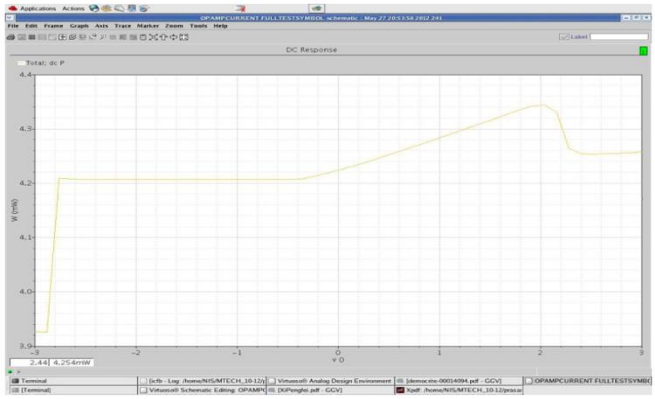

Fig 12: Power consumption of ping pong amplifier.

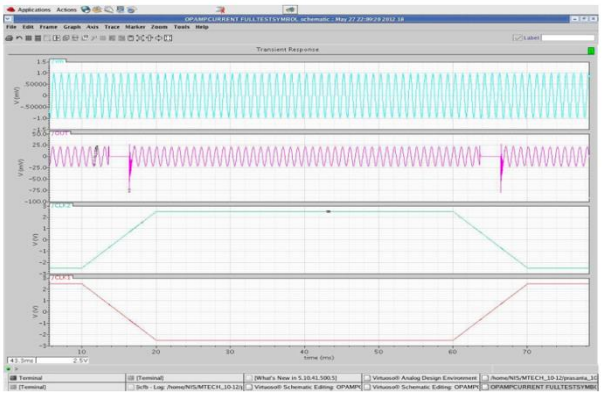

Fig 13: Discontinuity of output during clock transition

V. CONCLUSION

The design was tested for extremely low offset and automatic offset cancellation, and was successfully implemented. However, issues arose with ICMR, output range limitations, and output discontinuities. Additionally, improvements are still needed in gain and slew rate. Utilizing more precise switching and sample-and-hold (S&H) circuits, along with a folded cascode op-amp architecture, could lead to better performance.

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