Design and Analysis of Ripple Carry Adder and Carry Look Ahead Adder using Adiabatic Technology

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ABSTRACT: Adder is a unit block in the designing of the digital circuit design. Half adder and Full adder is mostly used in the addition and addition of product term in the multiplication. Mostly Ripple carry adder and Carry Look Ahead adder is used for addition of four bits. RCA consumes the least power but is the slowest (propagation delay is the most) while the CLA is the fastest but requires more power. A CLA is designed using the reversible Adiabatic logic which results in the power consumption as well as the propagation delay in a practical and usable range and is preferred over RCA and other adders.

KEYWORDS: Full Adder, Ripple Carry Adder, Carry look ahead Adder, Adiabatic logic.

I. INTRODUCTION

Adders can be designed using multiple techniques out of which Ripple Carry Adder (RCA) and Carry Look-ahead Adder (CLA) are considered for comparison based on their power and speed. In the designing of the digital circuits speed and power is conflict to each other. A Ripple Carry Adder consumes the least power but is the slowest (propagation delay is the most) while Carry Look-ahead Adder is the fastest but requires more power. Two full adders are implemented here – an RCA and a CLA – using CMOS technique, TG logic, GDI logic and Efficient Charge Recovery Logic (ECRL) adiabatic logic. Power consumption and propagation delay for these adders are compared at different operating frequencies and input voltages.

II. Basic Adder Blocks

2.1 Half Adder

Half Adder adds 2 single bits and produces a sum and carry bit that can be used for the next highest order bit. The circuit is created using the combination of an XOR and an AND Gate. Each gate handles a component of the output. The AND Gate takes the input and give the carry bit and the XOR gate outputs the sum bit.

$$\mathrm{SUM} = \mathrm{A} \oplus \mathrm{B}$$

$$\mathrm{Carry} = \mathrm{A} \bullet \mathrm{B}$$

Table 2.1 Half Adder Truth Table

Input		**Output**	
A	**B**	**Sum**	**Carry**
0	0	0	0
0	1	1	0
1	1	0	1

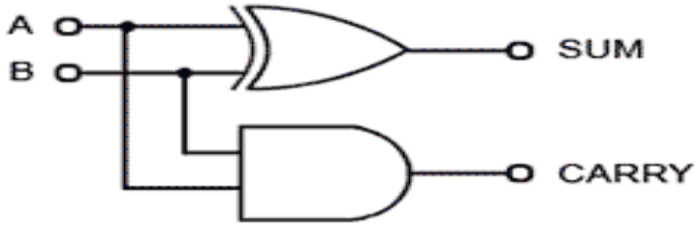

Fig 2.1 Half Adder Circuit

2.2 Full Adder

A Full adder is an extension of the half adder. This works by taking the carry bit from previous addition and using this along with the two input operand bits. This means that this adder can be used to add binary numbers with more than 1 bit [4]. Boolean equations for a full adder:

$$S = A \oplus B \oplus C$$

$$C_{out} = A \bullet B + B \bullet C_{in} + A \bullet C_{in}$$

Table 2.2 Full Adder Truth Table

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

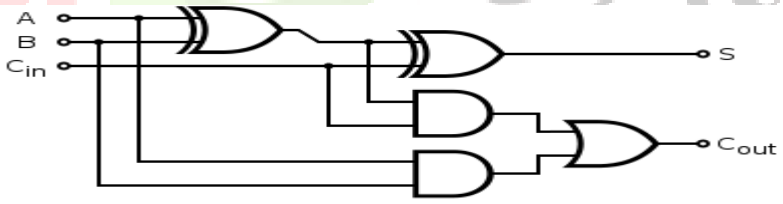

Fig 2.2 Full Adder Circuit

III. Multiple Bit Adders

3.1 Ripple-Carry Adder

A Ripple carry adder is designed using cascading connections of multiple full adders. A system of ripple-carry adders is a sequence of standard full adders that makes it possible to add numbers that contain more bits than that of a single full adder. Each full adder has a carryin (Cin) and a carryout (Cout) bit, and the adders are connected by connecting Cout on step n to Cin on step n+1 . The challenge with ripple-carry adders, is the propagation delay of the carry bits.

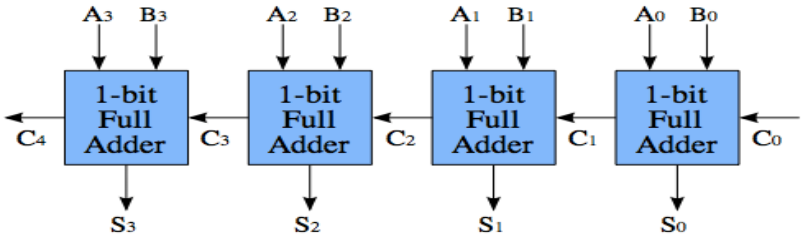

Fig 3.1 Ripple Carry Adder

3.2 Carry-Look ahead Adder

Carry-Look ahead adders (CLA) are the fastest adders, but they consumes maximum area. This adder is preferred for addition up to 4 bit length. A carry-lookahead adder system solve the problem of RCA, by computing whether a carry will be generated before it actually computes the sum. There are multiple schemes of doing this, so there is no "one" circuit that constitutes a look-ahead adder.The calculation of C4 is no faster than in the the ripple-carry above, nor is PG and GG - the magic only happens when you put several of these blocks together to add even larger numbers.The important to note part of the picture, is that the purple block is producing three values: C4, PG (Propagate) and GG (Generate). PG goes high if this block will propagate Cin to Cout, and GG goes high if the block will generate an overflow regardless of Cin. (Also, the block may neither propegate nor generate a carry, in which case both PG and GG are low, and Cout is 0.) PG and GG can be calculated in the purple block regardless of the value of C0 - thus, when C0 finally arrives, the purple block can simply consult its previously calculated result, and if the result is a "propagate," then C0 is propagated directly to C4; this is four times faster than propagating through all the four full adders.The reason why the block has the outputs PG and GG is so that, in a hierarchal fashion, we can acquire even greater propagation speedups.

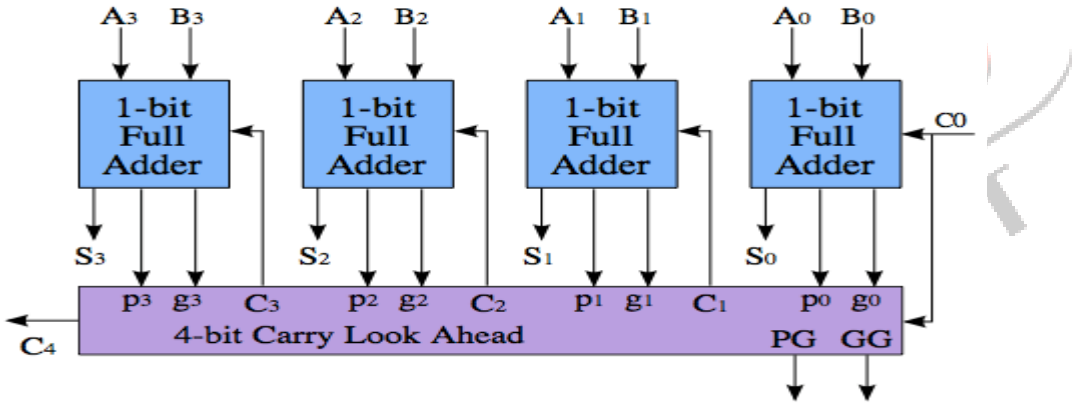

Fig 3.2 Carry Look Ahead Adder

IV. IMPLEMENTATION

4.1 Full Adder using CMOS

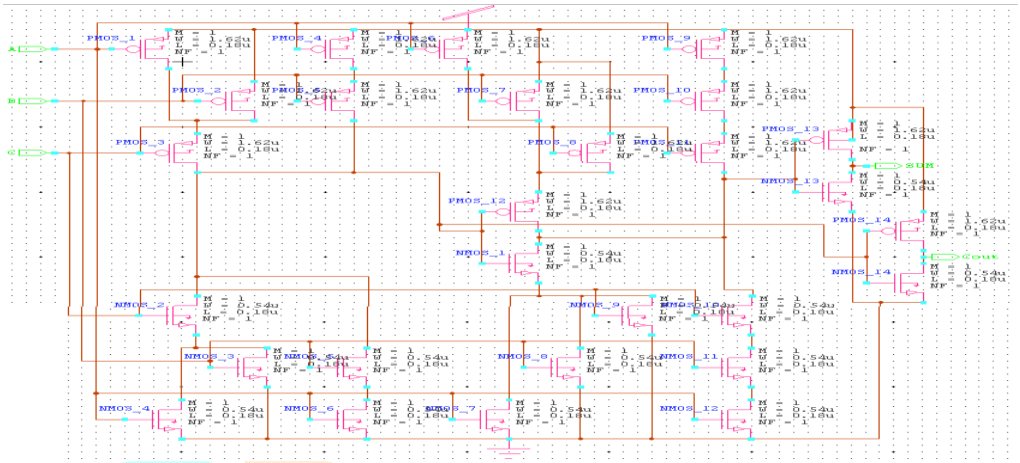

Fig 4.1 Full Adder using CMOS technology

4.2 Full Adder Using ECRL

Energy Charge Recovery Logic is an Adiabatic logic technique that is used to recover the power in a circuit or feedback power to the main power supply. An ECRL full adder consists of 2 cross-coupled transistors for each circuit for recovery. The pull-down network in the circuit uses NMOS transistors to design the logic circuit [5].

There are 4 phases in a typical ECRL circuit working – Precharge, Hold, Discharge & Recovery Phase.

1. During the Precharge phase, the pull-up network does some work while the pull-down network doesn't conduct and remains idle.
2. In the Hold phase, the outputs hold the valid logic levels and this condition is maintained throughout the phase.
3. As the circuit enters the Discharge and Recovery phases, the sum returns all the power it holds to the supply voltage.

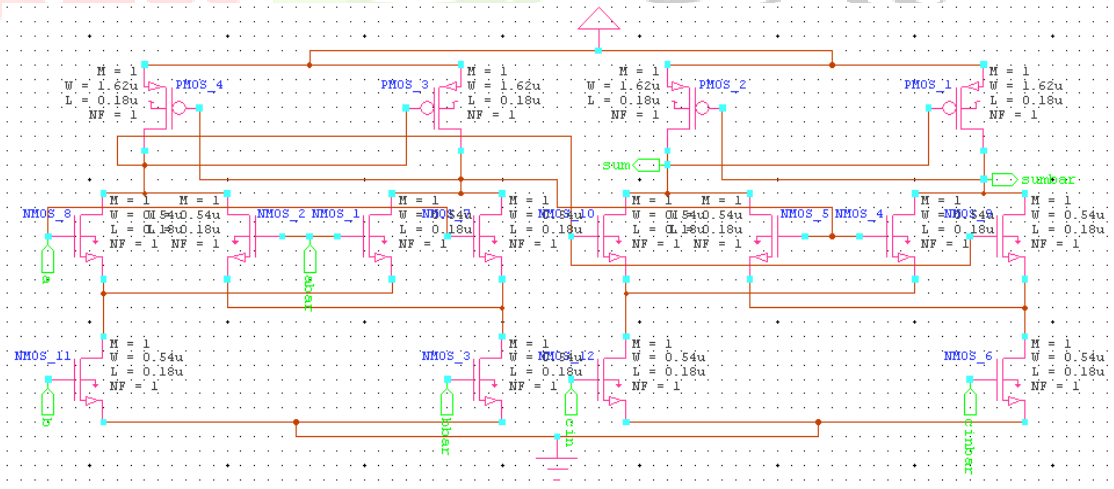

Fig.4.2.1. Sum circuit using ECRL logic

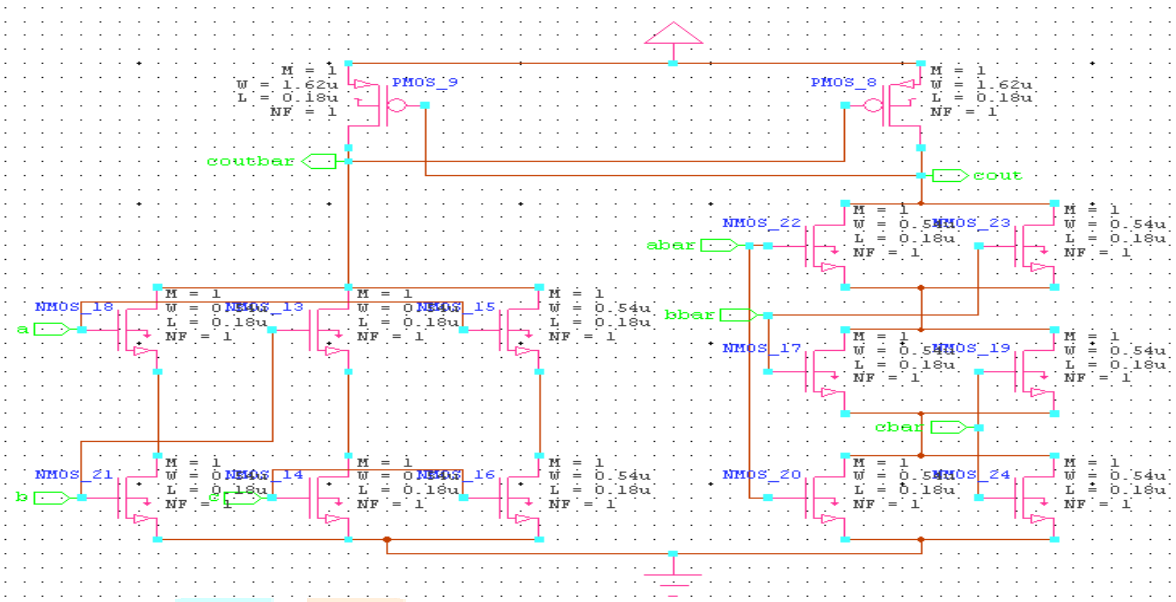

Fig.4.2.2. Carry circuit using ECRL logic

4.3 8-Bit CLA Using Transmission Gate (TG) Logic

CLA based on Conventional CMOS design uses a large number of transistors, and therefore consumes more power. A TG logic is used to reduce this transistor count and the power dissipation [2].

For designing a 1-bit adder based on TG logic, the circuit components used are - 2 XOR gates and a boolean expression logic, $g_i + p_i.c_i$, circuit. The design of these circuit components is different from the way it is done in Conventional CMOS design. 1 TG based full adder has 11 PMOS and 11 NMOS transistors.

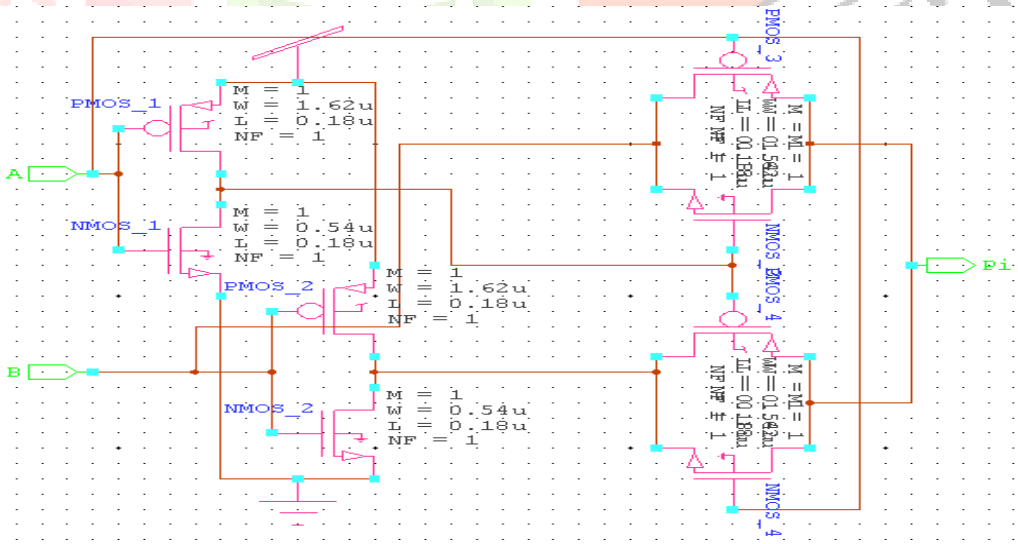

Fig.4.3. XOR gate using TG logic

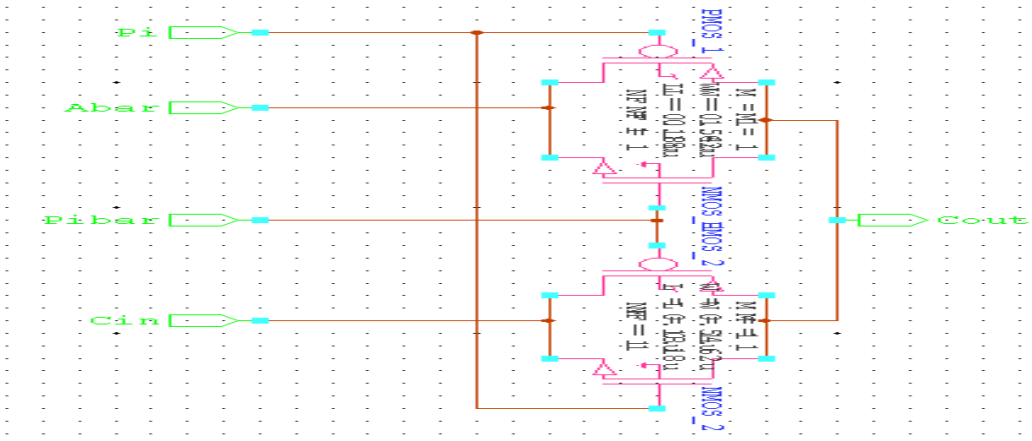

Fig.4.4.Carry Signal Generation using TG logic

4.4 8-Bit CLA Using ECRL Adiabatic Logic

To further reduce the power dissipation in a CLA, a technique named Adiabatic logic is used. A special case of which is Efficient Charge Recovery Logic (ECRL).To design a 1-bit adder using ECRL [1], 2 XOR gates, 1 AND gate and a (g_i + p_i.c_i) boolean expression logic circuit are used. It comprises of 11 NMOS and 25 PMOS transistors which is greater than that required in an RCA[6].

Here are the sub-circuits of a 1-bit ECRL adder-

1. **XOR Gate-** Fig.4.4.1 shows an XOR gate using ECRL with 2 PMOS and 6 NMOS transistors. The transistors PMOS_1 and PMOS_2 are used for precharge and recovery phase while the 6 NMOS transistors are used to design the XOR and XNOR logics.

NMOS_1, NMOS_2, NMOS_3 and NMOS_6 are used for the XNOR logic, which is:

$$\bar{a} \bullet \bar{b} + a \bullet b$$

and NMOS_4, NMOS_5, NMOS_6 and NMOS_2 are for the XOR logic

$$\bar{a} \bullet b + \bar{b} \bullet a$$

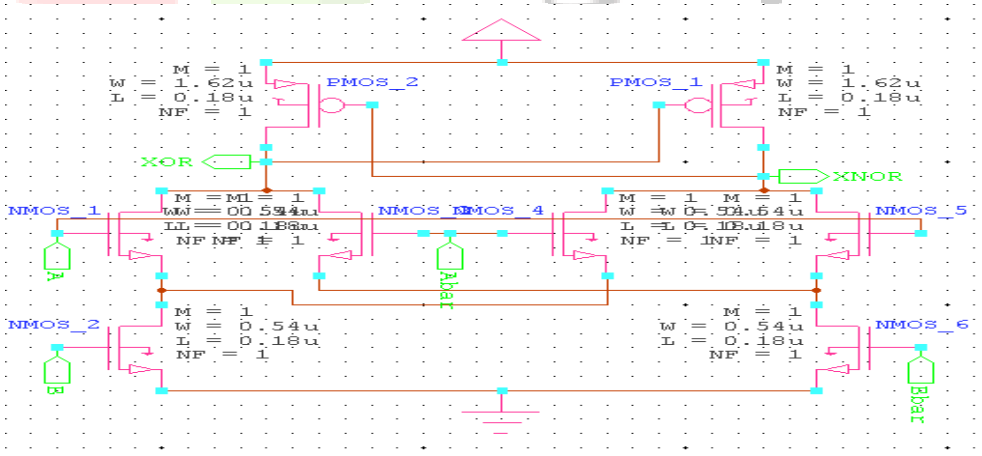

Fig.4.4.1 XOR gate using ECRL logic

2. **AND Gate-** Fig.4.4.2 shows an AND gate designed using ECRL adiabatic logic created from 2 PMOS and 4 NMOS transistors. The PMOS transistors are used in the precharge and recovery phase while the NMOS ones are used for the AND logic generation.[3]

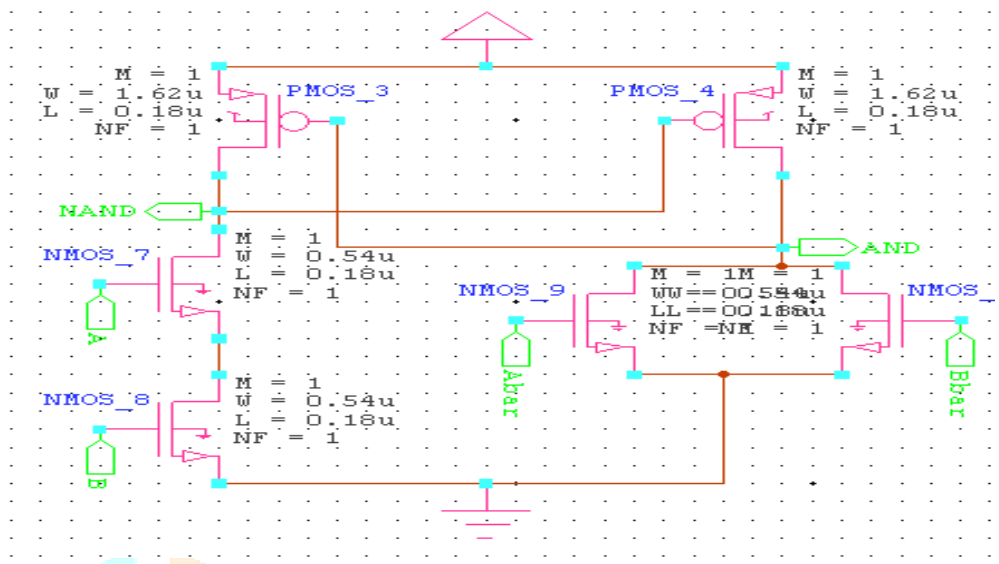

Fig.4.4.2. AND gate using ECRL logic

3. **Carry Signal Generation-** Fig.4.4.3 shows the carry logic circuit for ECRL.

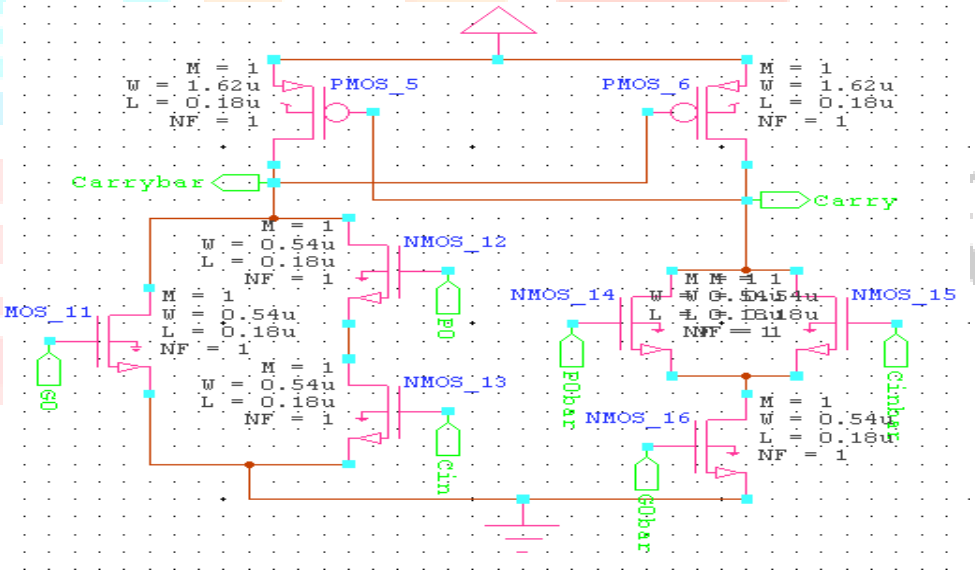

Fig.4.4.3. Carry Signal Generation using ECRL logic

Fig.4.4.3 shows an 8-bit CLA using the Adiabatic ECRL technique. It uses 88 PMOS and 200 NMOS transistors. Though the transistor count is greater here, the overall power dissipations is lesser because of the recovery phase of the circuit wherein the power from the supply is recovered and is used as a feedback to the circuit.

V. RESULT, ANALYSIS AND COMPARISON

The design and simulations have been done using Tanner Tools 15.23.Comparison of the propagation delay and the power dissipation for different full adders is shown at varying supply voltages and operating frequencies. An RCA is designed using Conventional CMOS, TG logic and ECRL techniques and a CLA using Conventional CMOS, TG logic,and ECRL. All the simulations are carried out at 180nm technology, NMOS transistor W/L ratio – 540/180 and PMOS transistor W/L ratio 1620/180.

5.1 Comparative Analysis of 8-Bit RCA and CLA

By analysing 8bit RCA and CLA for different logic design for different input voltages and frequency we can see that RCA is better in terms of power consumption but delay is very high. Due to this reason, a CLA is used. To reduce the drawback of CLA power consumption we have used adiabatic logic in this work so power level decreases as in RCA circuit

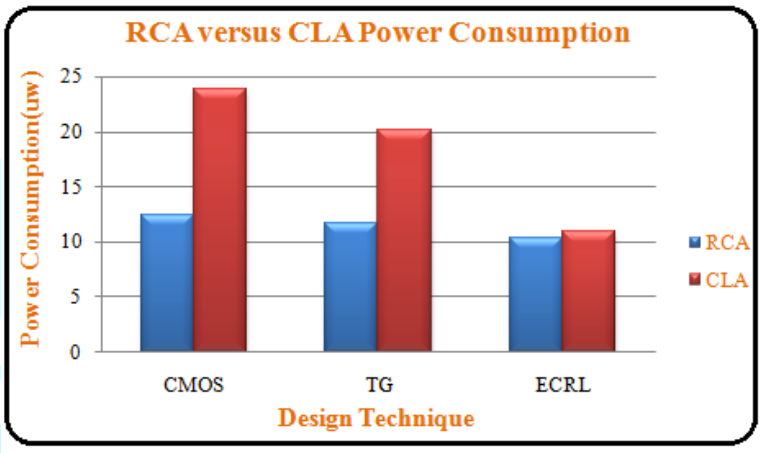

Fig.5.1.1 Power consumption for CLA and RCA

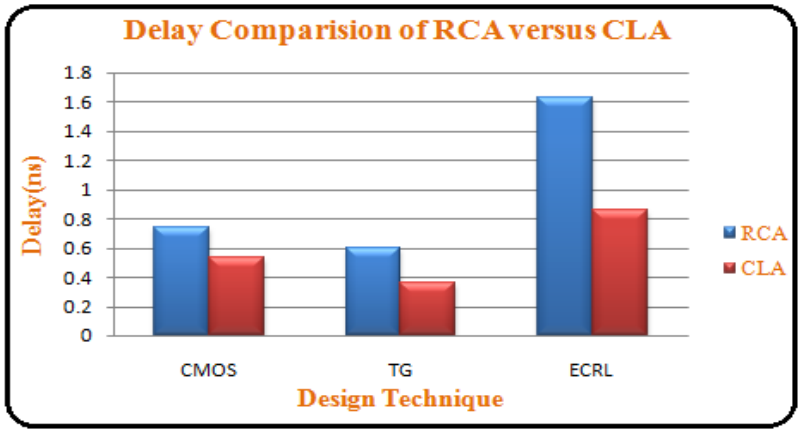

Fig.5.1.2 Delay comparison of RCA and CLA

VI. CONCLUSION

When we compare Ripple Carry Adder and Carry look ahead Adder, CLA is better compare to RCA.CLA is better from RCA using ECRL adiabatic logic in which delay is comparatively less.

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