Analytical Modeling and Scaling of the Suspended-Gate FET (NEMFET) for Low-Power Logic

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ABSTRACT

Power dissipation is a key factor for mobile devices and other low power applications. Complementary metal oxide semiconductor (CMOS) is the dominant integrated circuit (IC) technology responsible for a large part of this power dissipation. As the minimum feature size of CMOS devices enters into the sub 50 nanometer (nm) regime, power dissipation becomes much worse due to intrinsic physical limits. Many approaches have been studied at device and circuit level to reduce power dissipation of deeply scaled CMOS ICs. However, these approaches have unavoidable drawbacks which affect the performance as well as cost of device. Therefore, there is a strong need to find an emerging technology, which has nearly zero leakage current, but has high drive current, that also can utilize CMOS fabrication and design concepts, and can be integrated with CMOS technology without additional overhead. This paper focuses on the analysis, design, characteristics and applications of MOSFET replacement devices, with emphasis on the suspended gate FET (SGFET). Recently, the suspended-gate MOSFET (SG-MOSFET) was investigated as a possible candidate for ultra low power devices on the basis of numerical simulation and analytical modeling. Here, the comparison study is made between the SGFET structure which has been reported earlier and the new structure in which the dimensions are scaled to analysis the characteristics of scaled SGFET for ultra low power devices.

Key Words: Nano electro-mechanical field-effect transistor (NEMFET), suspended-gate FET (SGFET), device modeling, low-voltage, low-current.

INTRODUCTION:

Recent interest in so-called suspended-gate FET (SG-FET) devices has been motivated by their ability to offer solutions for ultra-low power logic, power management and capacitor-less memory devices by taking advantage of MEMS technology and properties. Today, MEMS technology has achieved a certain level of maturity and applications of RF MEM switches and resonators are foreseen in mobile communications and airborne or space electronics. Moreover, MEMS devices can be integrated monolithically with conventional CMOS devices using top-down surface micromachining processes, enabling novel functionality and performance together with low power consumption (based on electrostatic or piezoelectric actuation). MEMS passive elements, switches, and resonators are some of the most successful examples in the field.

DEVICE STRUCTURE:

Suspended-gate FET or SGFET also called NEMFETs closely resemble conventional MOSFETs. The main difference is the gate configuration; instead of being in direct electrical contact with the gate oxide, NEMFET gates are mechanically suspended as shown in Fig. 1. This introduces an air gap between the gate oxide and the gate and part of the gate voltage is dropped over the gap capacitance (C_{gap}). When the NEMFET is designed such that the mechanical pull-in occurs before a surface inversion layer forms, switching with a very sharp slope becomes possible.

A Micro- or Nano-Electro-Mechanical Field Effect Transistor (MEM- or NEM-FET) combines features of a pure NEM relay and a MOSFET: it has a movable part and a solid state semiconductor part that operate to couple the mechanical movement with the formation of the inversion/accumulation channel at the gate-insulator/semiconductor interface.

OPERATION AND ANALYTICAL MODELING:

The 3-D structure, 2-D cross-section, equivalent capacitor circuit, and symbol of the n-channel SGFET are shown in Fig.1. The dimensional parameters are defined as follows: L is the SGFET channel length, h is the thickness of the suspended gate (SG), t_{ox} is the gate-oxide thickness, t_{gap0} is the initial gap thickness, and W is the SGFET channel width that can be assumed equal to the beam (suspended bridge) length if $W >> t_{gap0}$; the beam width is equal to channel length L.

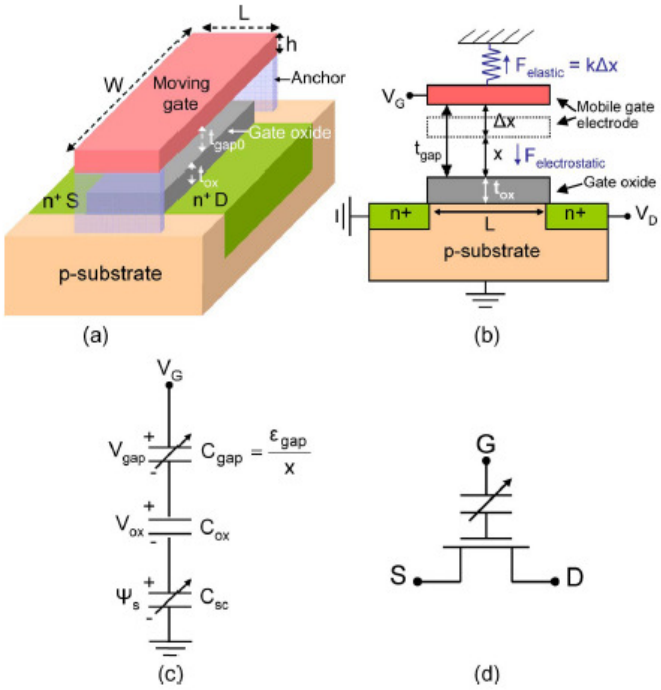

Fig. 1: N-channel SGFET. (a) Three-dimensional structure: The channel width is equal to the beam length (W = WFET = L beam), and the channel length is equal to the beam width (L = LFET = W beam). (b) Cross section parallel to device length. (c) Equivalent capacitor circuit. (d) Symbol [1].

An SGFET combines an electrostatically actuated NEMS switch and an inversion-mode MOSFET (Fig. 1). It is distinguished from a regular MOSFET by the presence of an air gap between the doubly clamped gate electrode and the gate oxide. The SG structure in Fig.1(a) is usually realized by the sacrificial etching of a material (such as cured polyimide, polycrystalline, or amorphous silicon) that is deposited on the gate insulator before the gate formation. The SG material is typically polysilicon or aluminum (AlSi). The bottom range of the values reported so far for the SGFET air gap is around a few hundred nanometers (approx. 130 nm minimum). An important challenge regarding the fabrication of SGFETs featuring CMOS-compatible actuation voltages is to realize both the gap and the gate electrode in the 10-nm range. Atomic-layer deposition seems a very promising technique for both structural and sacrificial layers, due to its monolayer-level thickness control, and can be used for fabricating SGFETs with vertical or lateral dimensions controlled at the atomic scale. It is important to mention that gap values below 10 nm were already demonstrated in biosensors; however, the layer over the gap was much thicker and not movable. On the other hand, fully released and functional h = 20 nm-thick nanocomposite Al–Mo resonators were also reported.

The operation of the SGFET is explained as follows: At flat band condition, (V_G = V_{FB}), the charge density at the gate electrode and inside the semiconductor is zero, yielding $x = t_{gap0}$, where x shows the actual distance between the gate oxide and the gate electrode [Fig.1(b)]. As V_G increases, a positive charge (and also an equal amount of negative charge inside the semiconductor) is built up in the gate electrode, giving rise to an electrostatic force pulling down the SG and resulting in $x < t_{gap0}$ [Fig. 2(a)].

Until the gate voltage reaches the "pull-in voltage" V_{pi}, the electrostatic force can be balanced by the counteracting elastic force. However, for $V_G \geq V_{pi}$ (corresponding to a critical surface potential $\Psi_s = \Psi_{pi}$ and a critical gap thickness x_{pi}), the electrostatic force overcomes the elastic component, and the gate collapses (is pulled in) on the gate oxide [Fig. 2(b)]. When the gate is pulled in, the abrupt increase in gate capacitance leads to an abrupt reduction of the threshold voltage and, consequently, a sharp increase in the drain current. As will be detailed later, the SGFET features mechanical hysteresis, which means that the pull-out of the SG requires a "pull-out voltage" $V_G = V_{po}$ that is lower than V_{pi}. In the following, the SGFET pull-in and pull-out voltages will be separately modeled, and an explicit relationship between the gate position and the gate voltage will be developed.

Pull-In Modeling:

When the electrostatic force exceeds the mechanical restoring force, this causes the top electrode to collapse onto the oxide layer and the corresponding voltage is the **pull-in voltage.**

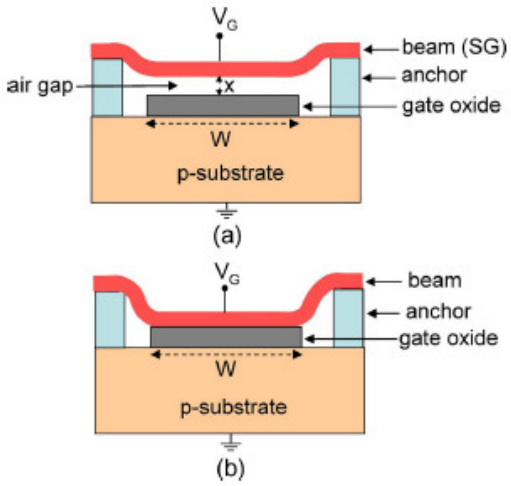

Fig. 2: Cross-section of the n-channel SGFET parallel to device width. (a) gate up ($V_{FB}<V_G<V_{pi}$, $t_{gap0} > x > x_{pi}$). (b) gate down($V_G \geq V_{pi}$, x = 0)[1].

We start with the force-balance equation related to the SG.

$$\frac{WL\varepsilon_{gap}V_{gap}^2}{2x^2} = k(t_{gap0} - x). \qquad (1)$$

The left-hand side of (1) designates the electrostatic attraction force applied to the SG, whereas the right-hand side designates the counteracting elastic force [Fig. 1(b)]. ϵ_{gap} is the gap permittivity, and V_{gap} is the voltage drop across the gap. The elastic force is represented by a linear spring constant k. This is a simplified assumption since the nonlinear stretching component of the spring constant, which can lead to a non negligible restoring force (and can alter the pull-out behavior), is neglected.

In (1), the vander Waals attraction between the SG and the substrate is not taken into account. However, it is worth mentioning that the impact of the vander Waals forces on the SGFET characteristics becomes non negligible if the air gap is extremely scaled: As an example, for $t_{gap0} \leq 2$ nm and $V_{gap} = 1$ V, the vander Waals forces are theoretically even higher than the electrostatic force.

V_{gap} is expressed as a function of the actual gap thickness and the V_G-dependent semiconductor charge density Q_{sc} as:

$$V_{\text{gap}} = -\frac{Q_{\text{sc}}}{\varepsilon_{\text{gap}}/x}. \qquad (2)$$

The denominator of (2) shows the actual gap capacitance per unit area, C_{gap} [Fig. 1(c)]. The substitution of (2) into (1) yields

$$x = t_{\text{gap0}} - \frac{WL}{2\varepsilon_{\text{gap}}k}Q_{\text{sc}}^2. \qquad (3)$$

Note that the second term on the right-hand side of (3) corresponds to the gate displacement Δx [Fig. 1(b)]. Equation (3) is valid for $x > x_{\text{pi}}$. Beyond this limit, the system is no longer in equilibrium, and the gate snaps down to the gate oxide, leading to $x = 0$. For a uniformly distributed electrostatic force along the beam and neglecting the residual stress, the spring constant k is given in terms of the structural parameters by

$$k = \frac{32ELh^3}{W^3}. \qquad (4)$$

In a simple MEMS switch, consisting of two parallel metallic plates separated by an air gap, the stability analysis yields $x_{\text{pi}} = 2t_{\text{gap0}}/3$. When a second capacitance C_f is connected in series with C_{gap}, x_{pi} is reduced to

$$x_{\text{pi}} = \frac{2 - C_{\text{gap0}}/C_f}{3}t_{\text{gap0}} \qquad (5)$$

where $C_{\text{gap0}} = \varepsilon_{\text{gap}}/t_{\text{gap0}}$ is the minimum gap capacitance. C_f induces a negative feedback on V_{gap} and is normally used to increase the travel range of the moving electrode in MEMS switches. Note from (5) that, for $C_{\text{gap0}}/C_f \geq 2$, the instability (i.e., pull-in) is completely suppressed. In the case of the SGFET, C_f is equal to the series equivalent of C_{ox} with C_{sc} [Fig. 1(c)]. Simple relationships for the pull-in voltage V_{pi}, the SG position at pull-in, x_{pi}, and the surface potential at pull-in (Ψ_{pi}) are obtained starting from the depletion approximation. Since our ultimate goal is to use the SGFET in logic circuits by taking advantage of the sharp on–off transition, we are naturally interested in the case where the pull-in (and hence pull-out) occurs before the formation of the inversion channel (this implies that $\Psi_{\text{pi}} < 2\Phi_F$, where Φ_F is the substrate Fermi potential). Therefore, in terms of our objective, the depletion approximation does not lead to a limitation.

Although SGFETs can be designed in such a way that the gate is pulled-in in the strong inversion region, this case exacerbates the short-channel effects due to the weak gate-to-channel coupling in the OFF-state and, therefore, will not be considered here. By contrast, the occurrence of the pull-in in weak inversion enables to suppress short-channel effects since the threshold voltage and the subthreshold swing are determined by the mechanical pull-in of the gate. As will be shown in the next section, the weak inversion switching allows the SGFET to eliminate the usual subthreshold region, where the slope of the current–voltage characteristic is finite, and to reduce the threshold voltage without increasing the off-current.

Using the depletion approximation, the depletion charge is given as a function of the surface potential by

$$Q_d(\Psi_s) = -\sqrt{2\varepsilon_{\text{Si}}qN_A\Psi_s} \qquad (6)$$

Where ε_{Si} is the silicon permittivity, q is the elementary charge, and N_A is the substrate doping. Substituting (6) into (3) for Q_{sc}, the gate position is expressed as a function of the surface potential

$$x(\Psi_s) = t_{gap0} - \frac{WL\varepsilon_{Si}qN_A}{\varepsilon_{gap}k}\Psi_s. \qquad (7)$$

According to (7), as long as the substrate is in depletion, the gate position is a linear function of the surface potential. The limit gate position at pull-in (x_{pi}) is written in terms of the limit surface potential at pull-in (Ψ_{pi}) by using (5) and by expressing C_f as a series combination of the oxide capacitance C_{ox} and the semiconductor capacitance C_{sc} (in depletion, $C_{sc} = \varepsilon_{Si}/x_{di}$, where x_{di} is the depletion depth at $\Psi_s = \Psi_{pi}$)

$$x_{pi} = \frac{2 - (\alpha + \beta\sqrt{\Psi_{pi}})}{3} t_{gap0} \qquad (8)$$

where

$$\alpha \equiv \frac{C_{gap0}}{C_{ox}} \qquad (9a)$$

$$\beta \equiv C_{gap0}\sqrt{\frac{2}{\varepsilon_{Si}qN_A}}. \qquad (9b)$$

The surface potential at pull-in is expressed by replacing Ψ_s by Ψ_{pi} and x by the expression of x_{pi} [given by (8)] in (7), and solving the resulting quadratic equation for Ψ_{pi}

$$\Psi_{pi} = \frac{\xi + \beta\sqrt{2\xi - \beta^2}}{2\chi^2} \qquad (10)$$

where

$$\chi \equiv \frac{3WL\varepsilon_{Si}qN_A}{t_{gap0}\varepsilon_{gap}k} \qquad (11a)$$

$$\xi \equiv 2(1+\alpha)\chi + \beta^2. \qquad (11b)$$

Equation (10) is the largest of the two distinct roots of the quadratic equation, which provides an accurate x_{pi}. Equations (8) and (10) are the relationships expressing x_{pi} and Ψ_{pi}, respectively, in terms of the structural parameters, and they are valid for $0 \le \Psi_{pi} < 2\Phi_F$.

The pull-in voltage is defined as the gate voltage leading to $\Psi_s = \Psi_{pi}$. From the equivalent capacitor divider circuit in Fig. 5.1(c), the effective gate voltage can be expressed as the sum of the voltage drops across the gap (V_{gap}), across the gate oxide (V_{ox}), and on the semiconductor (Ψ_s)

$$V_G(\Psi_s) = V_{FB} - \frac{Q_{sc}(\Psi_s)x(\Psi_s)}{\varepsilon_{gap}} - \frac{Q_{sc}(\Psi_s)}{C_{ox}} + \Psi_s \qquad (12)$$

where V_{FB} is the flatband voltage related to the work function difference and the oxide charge density. Substituting $x(\Psi_s)$ by x_{pi}, $Q_{sc}(\Psi_s)$ by $Q_d(\Psi_{pi})$, and Ψ_s by Ψ_{pi} in (12), the pull-in voltage of the SGFET, provided that the switching occurs in the weak inversion, is expressed as

$$V_{pi} = V_{FB} + \overline{\gamma}\sqrt{\Psi_{pi}} + \Psi_{pi} \qquad (13)$$

where

$$\overline{\gamma} \equiv \gamma\left(1 + \frac{C_{ox}}{\varepsilon_{gap}/x_{pi}}\right) \qquad (14)$$

And $\gamma = (2\varepsilon_{Si}qN_A)^{0.5}/C_{ox}$ is the usual MOSFET body effect coefficient. The term inside the parenthesis in (14) corresponds to the increase in capacitance once the gate is pulled in. Equation (13) is a general relationship for V_{pi}. It reduces to the well-known pull-in voltage of the simple NEMS switch, $V_{pi\ (sw)}$, for $N_A \rightarrow \infty$ (metallic bottom electrode case, leading to $\Psi_{pi} \rightarrow 0$ and $x_{pi} \rightarrow (2 - \alpha)\ t_{gap0}/3$) and $V_{FB} \rightarrow 0$ (same material for both electrodes):

$$\lim_{\substack{N_A \rightarrow \infty \\ V_{FB} \rightarrow 0}} V_{pi(SGFET)} = V_{pi(sw)} = \sqrt{\frac{8k(t_{gap0} + t_{ox}/\varepsilon_r)^3}{27\varepsilon_{gap}WL}}. \quad (15)$$

In (15), ε_r is the dielectric constant of the gate oxide material.

Pull-Out Modeling:

To restore the top electrode to its non-contacting or open state position, the applied voltage needs to be reduced below another critical voltage defined as the **pull-out voltage**.

In this section, we present a simple relationship for the SGFET pull-out voltage, starting from the forces acting on the gate while the gate is pulled in. We take into account the restoring elastic force and the opposing electrostatic and adhesion forces.

In the SGFET, once the gate is pulled in, the gate capacitance increases abruptly, and so do the surface potential and the charge density. The abrupt increase in charge density can also be explained by the abrupt reduction of the threshold voltage. For $V_G > V_{pi}$, the SGFET behaves as a conventional MOSFET. When V_G is swept back from a larger value than the pull-in voltage, pull-out does not occur at $V_G = V_{pi}$ because the surface potential is higher than Ψ_{pi}. This leads to a higher charge density and, to a higher electrostatic force than those at the onset of pull-in (while $x = x_{pi}$). The release of the gate is also retarded (if not completely prevented) by the surface adhesion forces. Therefore, V_G should be reduced to $V_{po} < V_{pi}$ in order for pull-out to happen.

The force-balance equation in the gate-down state, just before the pull-out, can be approximated in the first order as

$$\frac{WL\varepsilon_{ox}V_{ox}^2}{2t_{ox}^2} + F_a = kt_{gap0} \quad (16)$$

where the first term on the left-hand side represents the electrostatic force applied to the gate, whereas the term on the right-hand side shows the elastic restoring force of the doubly clamped beam. F_a is the surface adhesion force. In (16), we assumed that the spring constant is given by (4) even after the gate is pulled in [Fig. 2(b)]. The restoring elastic force can be more accurately calculated by taking into account the influence of the nonlinear stretching component on the spring constant. Furthermore, we neglected the peeling of the gate when V_G is swept back toward V_{po}, and we assumed that the gate stays in contact with the whole gate oxide area until the occurrence of the pull-out.

In the absence of capillary forces and at small roughness values, the adhesive interactions are dominated by the attractive vander Waals forces between non contacting surfaces rather than by the areas that are actually in contact. Due to the surface roughness, which prevents the intimate contact of dry MEMS surfaces, the adhesion energies are very low, typically in micro joules per square meter range. When the gate is in the down state, F_a can be expressed as

$$F_a \simeq 2WL\frac{\Gamma}{D_0} \quad (17)$$

where Γ is the interfacial adhesion energy per unit area. D_0 is an offset corresponding to the closest approach of the two surfaces and is determined by the average surface roughness. For $V_G = V_{po}$, the

depletion approximation leads to $V_{ox}/V_G=V_{po} = \gamma\Psi_{po}^{1/2}$, where Ψ_{po} is the surface potential at pull-out. From (16) and (17), Ψ_{po} is given by

$$\Psi_{po} = \frac{\varepsilon_{ox}}{\varepsilon_{Si} q N_A}\left(\frac{kt_{gap0}}{WL} - \frac{2\Gamma}{D_0}\right). \qquad (18)$$

Since $\Psi_{po} > 0$ for an n-channel SGFET, the condition

$$F_a < kt_{gap0} \qquad (19)$$

needs to be fulfilled in order for the beam not to stick to the substrate. In other words, in the absence of the electrostatic force (at flat band condition), the restoring force should be large enough to overcome the surface adhesion force.

The pull-out voltage is given as the sum of the flat band voltage, the voltage drop on the gate-oxide, and the surface potential at pull-out

$$V_{po} = V_{FB} + \gamma\sqrt{\Psi_{po}} + \Psi_{po}. \qquad (20)$$

Equation (20) stands as a general pull-out expression: It reduces to the pull-out equation of the simple MEMS switch featuring a dielectric layer for $N_A \to \infty$, $V_{FB} \to 0$, and $\Gamma \to 0$

$$\lim_{\substack{N_A\to\infty \\ V_{FB}\to 0 \\ \Gamma\to 0}} V_{po(SGFET)} = V_{po(sw)} = \sqrt{\frac{2kt_{gap0}t_{ox}^2}{\varepsilon_{ox} WL}}. \qquad (21)$$

It is worth mentioning that, besides the surface adhesion forces, the hysteresis window can also be enlarged by the oxide surface charge, whose density depends on the gate position (pulled in or pulled out). Indeed, this property is exploited in to build a capacitor less 1T memory cell. However, it is experimentally shown that this effect is mostly significant when the gate oxide is degraded, for instance, by an oxygen plasma process that induces traps on the oxide surface. More promising future SGFET memory architectures are likely to use controlled thin storage layers in the gate dielectric instead of the oxide traps; thin nanocrystal or ferroelectric layers can be engineered to achieve information storage in SGFET devices with relatively low operation voltages (< 5–10 V).

SG Position as a Function of Gate Voltage:

To obtain a relationship between the gate position and the gate voltage, (3) and (12) need to be solved together. However, the relationship resulting from these equations involves a third degree polynomial and does not provide a simple solution for $x(V_G)$ and $\Psi_s(V_G)$ even when the depletion approximation is used.

To obtain a simple, yet reasonably accurate expression for $x(V_G)$ yielding $x = t_{gap0}$ for $V_G = V_{FB}$ and $x = x_{pi}$ at $V_G = V_{pi}$, we first impose $x(\Psi_s) = x_{pi}$ in (12) and solve the resulting quadratic equation for Ψ_s while $Q_{sc} = Q_d$:

$$\Psi_{s,up} = \left(\frac{\overline{\gamma}}{2} - \sqrt{V_G - V_{FB} + \frac{\overline{\gamma}^2}{4}}\right)^2. \qquad (22)$$

Equation (22) is valid when the gate is in the up state and $V_G \le V_{pi}$. When the gate is pulled down and $V_G \ge V_{po}$, Ψ_s is given by the usual MOSFET relationship obtained by imposing $Q_{sc} = Q_d$ and $x = 0$ in (12) or by replacing γ in (22) by γ:

$$\Psi_{s,MOS} = \left(\frac{\gamma}{2} - \sqrt{V_G - V_{FB} + \frac{\gamma^2}{4}}\right)^2. \qquad (23)$$

Again, the quadratic equations providing (22) and (23) enable also a second root as solution, which is discarded since it does not correspond to the physical situation.
The expression for $x(V_G)$ is obtained by substituting (22) into (3) for Ψ_s while $Q_{sc} = Q_d$:

$$x(V_G) = t_{gap0} - \frac{WL\varepsilon_{Si}qN_A}{\varepsilon_{gap}k}\left(\frac{\overline{\gamma}}{2} - \sqrt{V_G - V_{FB} + \frac{\overline{\gamma}^2}{4}}\right)^2. \quad (24)$$

This analytical model provides insights related to the SGFET operation and basic design rules suitable for hand calculations. It develops simple relations for the pull-in and pull-out voltages, the travel range, and the SG position with respect to gate voltage. It also estimates the behavior and performance of the SGFET logic circuits.

Comparison of two configuration of SGFET:

With the help of analytical modeling, it has been proved that the suspended-gate field-effect transistor (SGFET) can be considered as a candidate to circumvent the limitation. Due to their extremely low standby power consumption and ideal switching characteristics, SGFETs can be used as sleep transistors for efficient power management and partitioning in highly scaled CMOS ICs. SGFETs can also be used to implement low-power (full-SGFET or SGFET/MOSFET) logic circuits. Here in this section, a comparison study is made between two different configurations of SGFET and also, pull-in and pull-out voltages, the travel range, and the SG position with respect to gate voltage is being calculated with the help of analytical model which has been discussed in earlier section. For the comparison of two SGFET, the parameters are taken as follows:

For SGFET 1:
L=100 nm, W=650 nm, h = 10 nm, t_{gap0} = 10 nm, t_{ox} = 2 nm, E=170 GPa, $\epsilon_{si} = 4.9*8.86*10^{-12}$ F/m, $\epsilon_{ox} = 11.7*8.86*10^{-12}$ F/m (For SiO_2), $\epsilon_{gap} = 8.86*10^{-12}$ F/m.

In second configuration, we take the lower value of width in comparison to first configuration or we decrease the width than it requires a corresponding vertical scaling (the reduction in t_{gap0} and/or *h* below 10nm) or the gate material with a smaller Young's modulus. So for the scaling of width, we take a smaller *h and* t_{gap0} values. Some other changes in other parameters are also made to make the same characteristics as of first SGFET. In second configuration we take the parameter as follows.

For SGFET 2:
L=100 nm, W=550 nm, h = 8 nm, t_{gap0} = 8 nm, t_{ox} = 3 nm, E=150 GPa, $\epsilon_{si} = 4.9*8.86*10^{-12}$ F/m
$\epsilon_{ox} = 9.7*8.86*10^{-12}$ F/m (For Si nano crystals), $\epsilon_{gap} = 8.86*10^{-12}$ F/m.

Variation of the surface potential as a function of the gate voltage:
With the help of Equation (3) and (12), the variation of the surface potential as a function of gate voltage is plotted for two different configuration of SGFET. Pull-in and pull-out voltages and their corresponding surface potential values are marked. Here $V_{pi,1}$, $V_{pi,2}$ are the pull-in voltages and V_{po1}, $V_{po,2}$ for SGFET 1 and SGFET 2 respectively. $\Psi_{pi,1}$ and $\Psi_{pi,2}$ are the surface potentials at pull in voltages and $\Psi_{po,2}$ and $\Psi_{po,2}$ are the surface potentials at pull-out voltages for both configurations of SGFET.

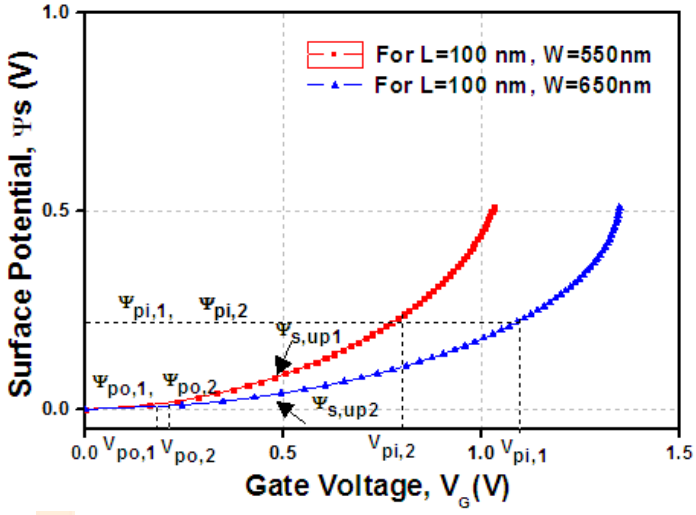

Fig. 3: Variation of the surface potential as a function of the gate voltage for two configurations of SGFETs.

For $V_G \leq V_{pi,1,2,}$ when the gate is in up-state we calculate the value of $\Psi_{s,up,1}$ and $\Psi_{s,up,2}$ which can be calculated with the help of Equation (22). With the graph it can be shown that the $\Psi_{s,up,1}$ value for SGFET1 is good agreement with $\Psi_{s,up,2}$ value for scaled configuration i.e. SGFET2 particularly for V_G values close to V_{FB} (since, for $V_G \approx V_{FB}$, $Q_{sc} \approx 0$, and sensitivity to x is very weak). The discrepancy between the two plot and for the gate voltage range $V_{FB} < V_G <$ Vpi is of minor importance, in the current voltage characteristics, the gate voltage range corresponds to the bottom of the subthreshold region with very low drain current values.

Variation of the normalized gap thickness as a function of the gate voltage:

With the help of Equation (24), the variation of the normalized gap as a function of gate voltage is plotted for two different configuration of SGFET. Note that the Equation (24), is valid for $x_{pi} \leq x(V_G) \leq t_{gap0}$. Graphs plotted for SGFET1 and SGFET2 are compared in Fig. 4 and both configurations produce the same trend. Also the pull-in and pull-out voltages are calculated from Equations (15) and (21) for both configuration.

Note that V_{FB} is assumed equal to zero in both configurations. For example, leading to $\Psi_s = 0$ in Fig. 3 and $x(V_G)/t_{gap0} = 1$ in Fig. 4 for $V_G = 0$.

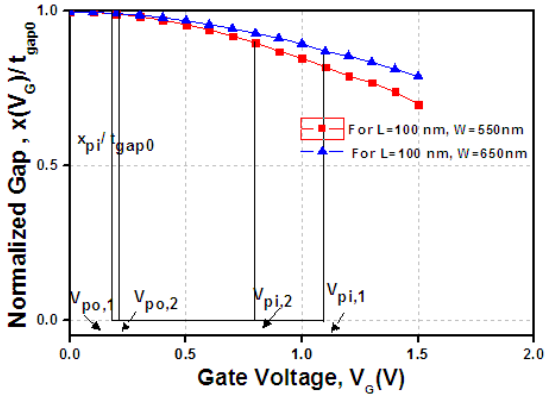

Fig. 4: Variation of the normalized gap thickness as a function of the gate voltage for two configurations of SGFETs.

Optimal design window for SGFET logic switches:

The use of SGFETs in logic circuits imposes the following conditions for the pull-in and pull-out voltages:

$$V_{po} > 0 \qquad (25a)$$

$$V_{pi} < V_{DD} \qquad (25b)$$

$$\Psi_{pi} < 2\Phi_F. \qquad (25c)$$

In addition to these, the threshold voltage when the gate is pulled in (the conventional MOSFET threshold voltage), $V_{T,\,MOS}$, should naturally satisfy

$$V_{T,MOS} = V_{FB} + \gamma\sqrt{2\Phi_F} + 2\Phi_F < V_{DD}. \qquad (25d)$$

The scaling of the supply voltage V_{DD} is normally imposed by (25b), rather than (25d), despite the high body doping that tends to increase $V_{T,\,MOS}$.

The impact of the structural parameters on the constraints mentioned earlier is shown in Fig. 5.5 (a)–(d) where the variation of the pull-in and pull-out voltages as a function of the (a) device width, (b) gap height, (c) SG thickness, and (d) gate material's Young's modulus is shown. Note that the dimensions used in Fig.5 is in the nanometer scale, and they are about three orders of magnitude smaller than the typical dimensions of MEMS switches (several micrometers for the vertical dimensions and hundreds of micrometers for the beam length) in order to meet the requirements of a small device footprint and a low-voltage actuation (the range of the parameters in Fig. 5 is selected such that $V_{pi} \leq 2$ V). As a general trend, both V_{pi} and V_{po} increase as the beam (SG) gets stiffer, i.e., as the spring constant increases by lowering W or increasing h or E. V_{pi} and V_{po} increase also for a larger t_{gap0} due to the lowered electrostatic force. For $t_{gap0} = h = 8$ nm and for a polysilicon SG ($E = 150$ GPa), sub-1 V operation ($V_{pi} - V_{FB} < 1$ V) requires roughly $W \geq 600$ nm. Further lateral scaling requires a corresponding vertical scaling (the reduction of t_{gap0} and/or h below 10 nm) or the use of a gate material with a smaller Young's modulus (Al or Ti). However, these solutions may not be viable due to the pronounced impact of the van der Waals forces (as $t$gap0 is reduced) and also due to the pull-out requirements. Fig. 5 reveals that an excessive increase of W or an excessive lowering of the t_{gap0}, h, or E may reduce the elastic restoring force (kt_{gap0}) to an intolerably low value, which could result in sticking according to (19).Therefore, the scaling of V_{DD} depends (indirectly) on the pullout characteristics as well. The maximum value of W and the minimum value of t_{gap0}, h, and E that would not lead to sticking (while the remaining parameters are fixed) correspond to $\Psi_{po} = 0$ [and hence to $V_{po} = V_{FB}$ according to (20)], and they are indicated with arrows in Fig. 5.

The strong sensitivity of V_{pi} and V_{po} with respect to the horizontal and vertical dimensions imposes a particularly tight process control to obtain uniform SGFET characteristics. The dependence of the pull-out (and hence the hysteresis window width) on the surface adhesion forces is the main technological challenge related to the fabrication and design of SGFETs. A reliable fabrication of SGFETs with a well-controlled pullout requires in-depth understanding and control of the surface adhesion forces.

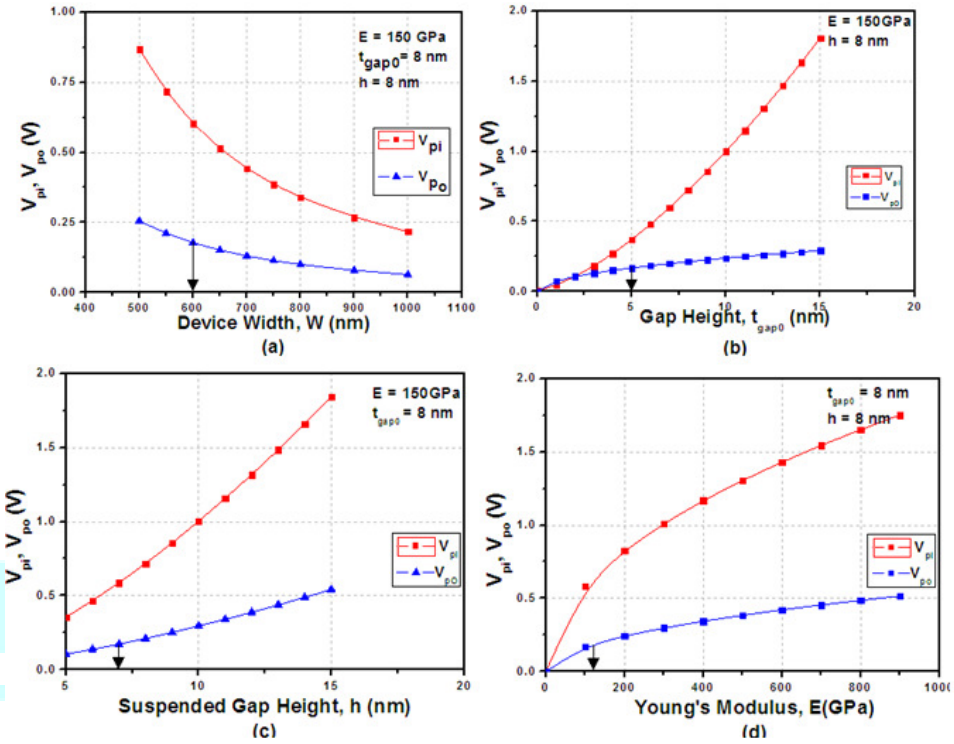

Fig. 5: Variation of the pull-in and pull-out voltages as a function of the (a) device width, (b) gap height, (c) SG thickness, and (d) Young's modulus of the gate material. L = 100 nm, t_{ox} = 3 nm (SiO2), N_A = 3.10^{17} cm−3, V_{FB} = 0.18 V, Γ = 20 μJ/m^2, D_0 = 0.2 nm, and $V_{T,\,MOS}$ = 1.4 V. The variation of V_{po} for $V_{po} > V_{T,\,MOS}$ is not shown since (20) is only valid in depletion.

SGFET performance, opportunities and limits:

Although truly nanometer-scale SGFETs have not been experimentally demonstrated to date, successful demonstrations of micron-scale devices together with simulations of scaled SGFETs with calibrated models indicate that SGFETs are promising for LSTP applications. In a first phase, SGFETs potentially could be an add-on to CMOS platforms for power management. In a later stage, after full assessment of their long-term reliability (including variability), they may become candidates for logic and/or memory functions. Based on experimental demonstrations to date, one could envision the SGFETs as a three- or four terminal binary switches (using charge or voltage as the state variable) which provides for 3-4 decades reduction in standby power as compared to the MOSFET. Its intrinsic speed could be of the order of GHz, with operating voltage below 1 V and switching energy on the order of aJ. Very recent reports on energy-reversible complementary NEM logic gates, demonstrate that for the same delay, energy-reversible architectures can operate at significantly lower supply voltage, which is beneficial for better reliability.

Beyond these applications, the SGFETs can offer unique analog/RF on-chip functions; as reported in, they can be used to efficiently transduce mechanical motion (*e.g.* a vibrating body) into an electrical signal (varying drain current), due to built-in gain. Low motional resistance (as low as 250 Ohms reported in) is required to enable ultra-scaled, low-power on-chip oscillators and RF blocks.

Conclusion and future scope:

Scaled SGFET static characteristics and design criteria were analyzed. Basic formulas for the pull-in and pull-out voltages were provided, and the SG position is explicitly expressed in terms of the gate voltage.

By using our model, key device parameters were highlighted, a considerable I_{on}/I_{off} ratio improvement in SGFETs is demonstrated, and the conditions for a low power and low-voltage operation are determined. Scaling of the SGFET into the deca-nanometer regime is one of the key requirements for its future success. Both the lateral (photolithographically defined) device dimensions and the thicknesses of the different layers, including the actuation air-gap, must be reduced together. Air-gaps on the order of 10 nm are feasible today; the smallest air-gap reported to date is 2-3nm between two gold lines, formed by depositing gold over a patterned resist trench. The benefits of scaling include reduced layout area for denser memory or logic functions (to be competitive with other technologies), lower actuation voltage (enabled by nanometer scale air-gaps) and higher operation frequency (as the device resonance frequency increases). Exploitation of suspended nanowire and nanotube technologies could enable SGFETs to operate at near-GHz frequency with negligible standby power consumption. The SGFET is particularly attractive as a power-gating device for high-performance CMOS platforms, because of its very high I_{on}/I_{off} ratio (3-4 decades larger than that for a MOSFET).

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