Design And Analysis Of Vedic Multiplier Using Full Swing Modified Gate Defused Input Method

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Abstract: The complexity in VLSI design increases with an increase in the level of integration. Due to the portable electronics area, power and delay have become the most important factors. In conventional CMOS design, the area, power and delay are more compared to other Low power techniques. In this paper Vedic multiplier is designed using different low power techniques, such as, conventional CMOS, GDI, Modified GDI, full swing defused gate style and hybrid structure which has a combination of GDI, TG, XOR, XNOR and pass transistor logic. All the designs are compared for area, power and delay. The power delay product graph is drawn for all the designs. The design and simulation are done in MENTOR GRAPHICS TOOL in 45 nm technology.

Keywords: **low power, GDI, modified GDI, hybrid full adder, mentor graphics, PDP, Vedic multipliers.**

I INTRODUCTION: The expanding greatness of compact gadget requests high chip thickness, low power utilization and ease. Decreasing the power utilization is the critical objective in the plan of advanced. Simple approach to meet this objective is to enhance the execution at the rationale levels. Regular advanced circuits were outlined utilizing reciprocal metal oxide semiconductors (CMOS)[1][2][6]. A new Low power VLSI outline system called GDI (Gate dissemination Input) is utilized as a part of the plan of advanced segments. This Technique has similarly more points of interest over the conventional CMOS plan. This paper gives similar examination in view of the execution of CMOS and GDI systems[4][6].

A Multiplier is the basic piece of the considerable number of processors. Subsequently a rapid and territory effective multiplier is required. Duplication operation is performed by the arrangement or parallel expansion ideas. Outline of adders with GDI method will enhance the execution of multipliers. But GDI method suffers from swing degradation. Here the 4x4 Vedic multiplier is designed using full swing modified GDI method.

II EXISTING SYSTEM AND PROBLEM STATEMENT: In spite of the fact that the GDI procedure lessens the transistor check, it experiences swing degradation because of numerous threshold loss. The XOR utilizing GDI is appeared in Figure 1. The yield of the GDI XOR entryway for every conceivable info is recorded in table 1. It demonstrates that when input B= „0‟ there is misfortune in yield of XOR gate. When the info A= “0” and B= “0” the transistors M1 and M3 are ON and the esteem B=”0‟ goes through M3, rather than „0‟ it will exchange VTP in light of the fact that P-transistor exchanges solid rationale “1‟ and powerless rationale “0‟. At the point when input A= “1” and B= “0‟ the transistors M1 and M4 are ON and the normal yield is VDD yet it will exchange VDD-VTN in light of the fact that N-transistor exchange frail rationale "1‟ and solid rationale 0.

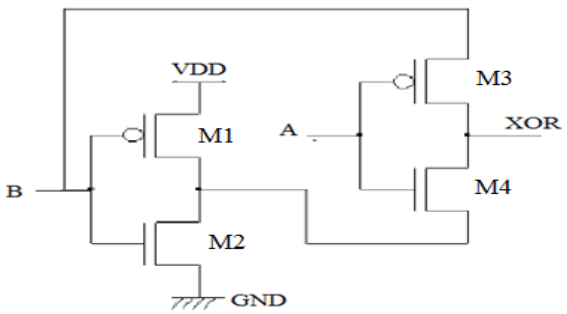

Fig 1: GDI XOR gate

Table 1: Swing degradation problem in GDI XOR gate

A	B	OUTPUT
0	0	V_{TP}
0	1	V_{DD}
1	0	V_{DD}-V_{TN}
1	1	0

In GDI 10 transistor full adder at the point when the sources of info ABC = "001", "010", "100","111" the Sum flag of the full viper experience the ill effects of swing debasement because of an multiple threshold loss.

III PROPOSED SYSTEM: 17T FULL ADDER USING FULL SWING GDI: This adjustment style of full adder requires 17 transistors. The swing degradation issue in 10T full viper is lessened by including extra 7 transistors. It utilizes swing reclamation (SR) transistor to accomplish full swing for both XOR doors in full snake. The XOR door with SR transistor is appeared in Figure

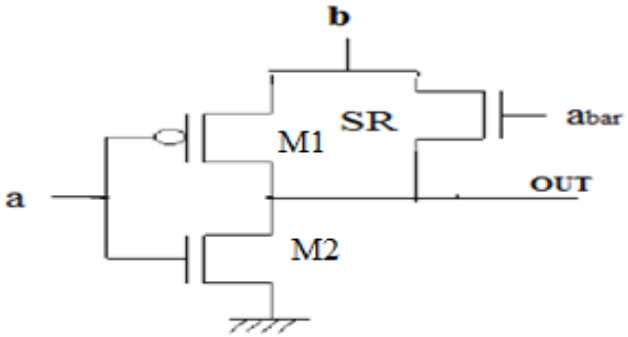

Fig 2: Modified full swing GDI XOR gate

In GDI XOR entryway, the swing corruption issue happens when the info AB= "00" because of the powerless rationale „0" exchange of P-transistor. To beat this issue an extra SR transistor (N-transistor) is utilized as a part of parallel with P-transistor. The source and deplete of SR transistor have an indistinguishable contributions from that of the P-transistor yet the door input is rearranged. The quantity of extra transistors required to accomplish full swing of GDI XOR are, 3 transistors for swing rebuilding and 4 transistors to reverse the door input. Altogether, it requires 17 transistors to configuration full swing changed GDI full snake. The outline of 17T full swing adjusted GDI full viper is appeared in Figure 3

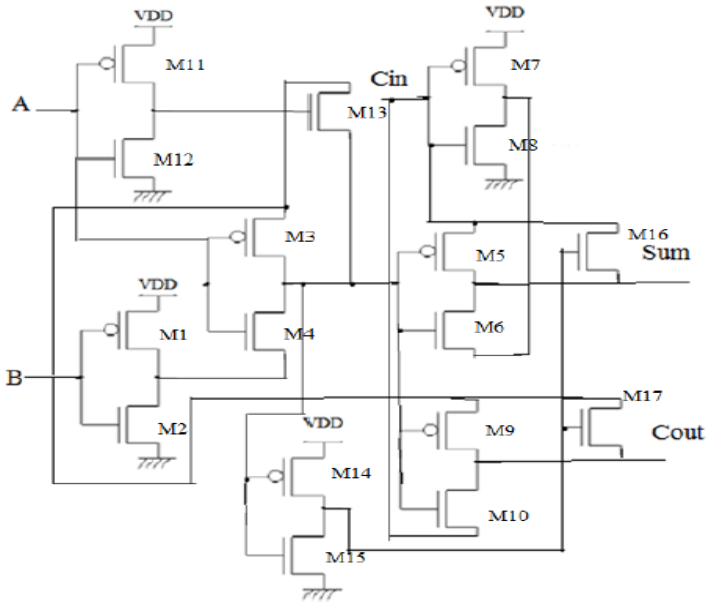

Fig 3: 1-bit Full adder using full swing modified GDI technique

IV 4X4 VEDIC MULTIPLIER USING FULL SWING MODIFIED GDI TECHNIQUE

Multipliers are composed with the assistance GDI based adders and a Vedic multiplication procedure called "Urdhva-Tiryakbhyam", Which can be utilized for decimal multiplication as well as for double multiplication[5][7][9]. This principally comprises of the parallel age of halfway items and playing out the expansion operation all the while. This calculation can be utilized for N×N bit multiplications. To outline this system, let us consider two decimal numbers 252 and 846 and the multiplication of two decimal numbers 252×846 is clarified by utilizing the line chart appeared in beneath figure 4.

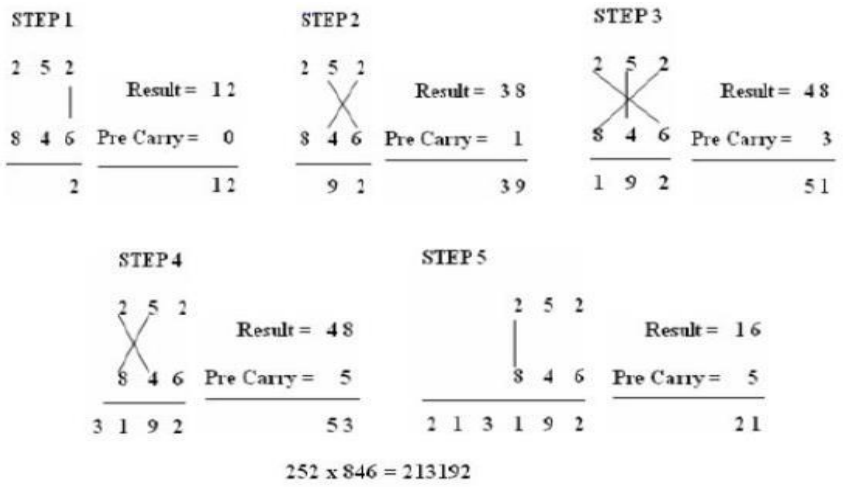

Fig 4: Multiplication of two decimal numbers using Urdhva-Tiryakbhyam suthra

Now consider two four piece numbers are An and B with the end goal that the individual bits are spoken to as the A3 A2 A1 A0 and B3 B2 B1 B0. The last yield is C6 S6 S5 S4 S3 S2 S1 S0. The halfway items are ascertained in parallel and subsequently delay is diminished immensely for the expansion in the quantity of bits. The Least Significant Bit (LSB) S0 is gotten effortlessly by duplicating the LSBs of the multiplier and the multiplicand.

Here the multiplication is taken after as indicated by the figure 4. In the wake of playing out every one of the means the outcome (Sn) and Carry (Cn) is gotten and similarly at each progression the past stage convey is sent to the following stage, and the procedure goes on

$S0 = A0B0$ -----(1)

$C1S1 = A1B0 + A0B1$ -----(2)

$C2S2 = C1 + A0B2 + A2B0 + A1B1$ -----(3)

$C3S3 = C2 + A0B3 + A3B0 + A1B2 + A2B1$ -----(4)

$C4S4 = C3 + A1B3 + A3B1 + A2B2$ -----(5)

$C5S5 = C4 + A3B2 + A2B3$ -----(7)

$C6S6 = C5 + A3B3$ -----(8)

The block diagram of 4x4 vedic multiplier is shown in the figure 5

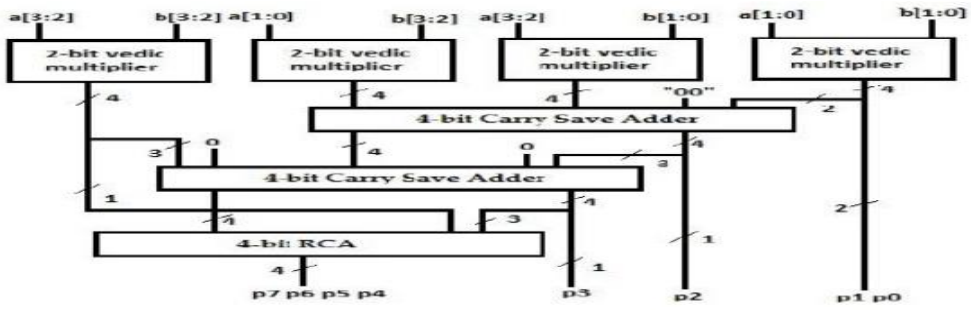

Fig 5: Block diagram of 4x4 vedic multiplier

V SIMULATION RESULTS

The design of 17 transistor full adder using modified full swing GDI technique is with W= 1um, L= 0.045um for P-MOS and W= 0.5um, L=0.045um for N-MOS, shown in Figure 6

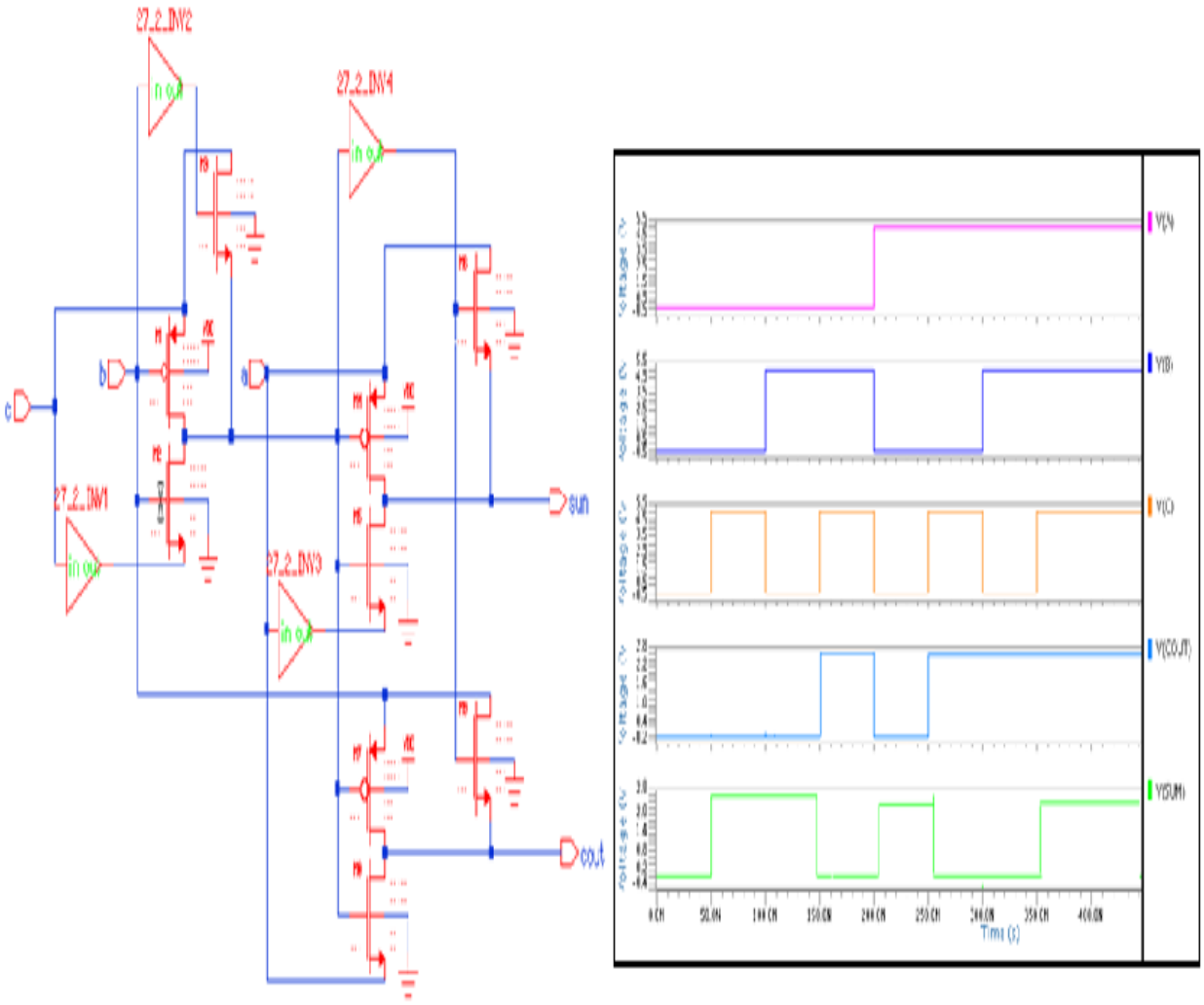

Fig 6: 1bit full adder using full swing modified GDI technique

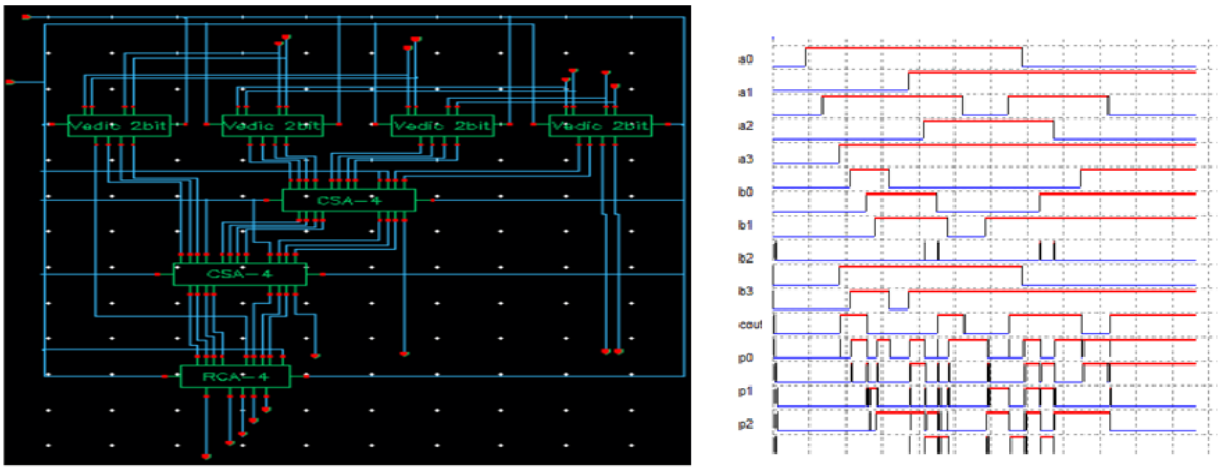

Fig 7: Design and simulation of 4x4 Vedic multiplier using modified full swing GDI technique.

VII RESULT ANALYSIS:

It shows that, the CMOS design requires large transistor count. The conventional GDI technique reduces the transistor count, but dissipates more power than the CMOS and it suffers from swing degradation.

The 17T full swing GDI technique eliminates output swing degradation by compromising transistor count and dissipates very less power compared to all other designs and it results full swing output.

Vedic Multipliers Designs are executed and mimicked utilizing 45nm Technology in Mentor Graphics at 1V Supply. Power Consumption and Delay are computed. Figure 8 demonstrates the Power utilization and Delay Comparison of Proposed Design with the current Vedic Multiplier Designs. In Vedic Multiplier utilizing Modified GDI there is 75% and 53.9% decrease in Power Consumption and Delay individually.

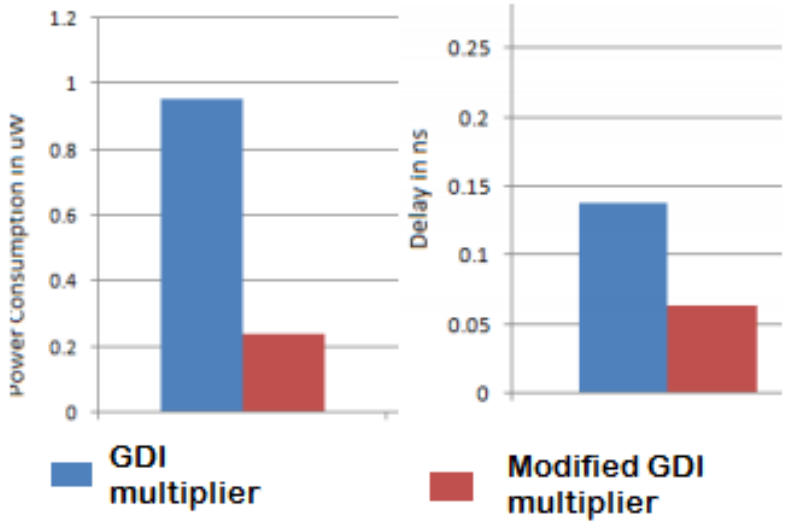

Fig 8: Power and delay comparison of modified GDI multiplier with conventional GDI multiplier

CONCLUSION

All the flag and information processing operations include multiplication. As speed is dependably a limitation in the duplication operation, increment in speed can be accomplished by decreasing the quantity of ventures in the calculation process. Vedic Multiplication includes less number of Steps. The speed of multiplier decides the proficiency of such a framework. In any framework plan, the three fundamental imperatives which decide the execution of the framework are speed, territory and power necessity. Utilizing Modified GDI Technique Low Power can be accomplished with less number of Transistors. The 4-bit Vedic Multiplier Designs are actualized utilizing Modified GDI system executed in Mentor graphics in 45nm process technology. The outcomes demonstrate execution is improved as far as Power and Delay.

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