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Design and Simulation of a 16-bit R–2R Ladder DAC in 130nm CMOS Technology

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Abstract: This paper presents the design and simulation of a 16-bit Digital-to-Analog Converter (DAC) using an R–2R ladder architecture implemented in 130nm CMOS technology. The DAC employs a two-stage operational amplifier for current-to-voltage conversion. The design is simulated using Cadence Virtuoso, and key performance parameters such as resolution and transient response are analyzed. The results demonstrate correct functionality while overcoming limitations due to mismatch and non-ideal effects.

***Index Terms* -** DAC, R–2R ladder, CMOS, 16-bit, Operational Amplifier, Mixed-Signal Design

I. INTRODUCTION

Digital-to-Analog Converters (DACs) are essential components in modern electronic systems, enabling conversion of digital signals into continuous analog outputs. High-resolution DACs are widely used in GPR systems, communication systems, audio processing, and instrumentation. Among various architectures, the R–2R ladder DAC is preferred due to its simplicity, scalability, and ease of implementation. In this work, a 16-bit DAC is designed using 130nm CMOS technology. DAC architectures are broadly classified into binary-weighted, thermometer-coded, and segmented types based on decoding techniques. Among physical implementations, resistor-based DACs, capacitor-based DACs, and current-steering DACs are widely used. Resistor ladder DACs, particularly the R–2R architecture, are popular due to their simplicity, scalability, and ease of implementation in CMOS technology. However, challenges such as resistor mismatch, noise, and nonlinearity (INL and DNL) affect their accuracy and performance. The proposed R–2R ladder DAC differs from conventional implementations in its integration with a carefully designed two-stage CMOS operational amplifier to improve output accuracy and stability. Additionally, the design is implemented in 130nm CMOS technology, allowing compact realization while maintaining adequate performance. The implementation also ensures monotonic behavior across the full input range, which is critical for high-resolution DAC performance.

II. LITERATURE SURVEY

Parmar and Gharge [1] proposed a 32-bit R–2R ladder DAC and analyzed its performance in terms of noise, resolution, and linearity. The study highlights that although R–2R DACs are cost-effective and simple to implement, they suffer from high INL and DNL errors due to resistor mismatch, leading to reduced accuracy. The authors also demonstrated that noise significantly impacts DAC performance, especially at high resolutions, where the Least Significant Bit (LSB) becomes extremely small. Simulation results showed that noise levels can exceed several LSBs, thereby degrading resolution. Rajendra Prasad et al. [2] designed a 4-bit R–2R DAC using 45 nm CMOS technology, focusing on low power consumption and improved linearity. The work integrates a two-stage operational amplifier to enhance gain and reduce INL and DNL errors. Sperotto et al. [3] introduced a MOS-only M–2M ladder DAC, which is a variation of the R–2R architecture optimized for ultra-low voltage (ULV) operation. Unlike traditional resistor ladders, the M–2M DAC uses MOS transistors to perform current division, enabling operation at supply voltages as low as 70 mV–140 mV.

Meyer et al. [4] presented a 12-bit R–2R ladder DAC implemented in 130nm CMOS technology for use in trapped-ion quantum computing systems, where precise analog waveform generation is critical. The DAC operates at a sampling rate of 1 MHz and is capable of generating multiple waveform types such as sinusoidal, triangular, and rectangular signals with a resolution of 500 µV.

III. R-2R LADDER DAC ARCHITECTURE

The R–2R ladder DAC offers several important advantages that make it one of the most widely used DAC architectures. It requires only two resistor values (R and 2R), which simplifies fabrication and ensures better matching compared to binary-weighted DACs. This structure is highly scalable, allowing easy extension to higher resolutions without needing a wide range of precise resistor values. Additionally, the R–2R DAC provides good linearity and monotonic behavior, making it suitable for accurate signal generation. It is also area-efficient and cost-effective, as it can be easily implemented in CMOS technology. Furthermore, its simple design and relatively constant output impedance make it convenient for integration with other analog circuits, such as operational amplifiers for improved performance.

The output voltage of the DAC is given by:

$$V_{\text{out}} = V_{\text{ref}} \cdot \frac{D}{2^N} \qquad (1)$$

The least significant bit (LSB) is:

$$\text{LSB} = \frac{V_{\text{ref}}}{2^{16}} \qquad (2)$$

The R–2R ladder network operates by successively dividing the reference voltage based on the digital input bits, where each bit contributes a weighted portion to the final output. The ladder structure ensures that the output impedance remains constant regardless of the input code, which is a key advantage over binary-weighted resistor DACs. This architecture simplifies implementation since only two resistor values are required, while still enabling high-resolution conversion. However, the accuracy of the DAC is highly dependent on precise resistor matching and switch performance, especially for higher resolutions such as 16-bit designs.

IV. OPERATIONAL AMPLIFIER DESIGN

The operational amplifier employed in this work is a two-stage CMOS amplifier designed to provide high gain, adequate bandwidth, and stable operation for accurate digital-to-analog conversion. The first stage consists of a PMOS differential input pair, which converts the differential input voltage into a corresponding current. This stage is chosen for its high transconductance. The differential pair is biased using a constant current source, ensuring stable operation and high input impedance. A PMOS current mirror is used as the active load, which performs differential-to-single-ended conversion while significantly increasing the output resistance and thereby enhancing the voltage gain of the stage. The second stage is implemented as a common-source amplifier, which provides additional voltage gain and improves the output driving capability of the op-amp. The overall gain of the amplifier is determined by the product of the gains of the individual stages, enabling the design to achieve sufficiently high open-loop gain required for precision DAC operation. To ensure stability, a Miller compensation capacitor is connected between the output of the second stage and the intermediate node of the first stage. This introduces a dominant pole and improves the phase margin, preventing oscillations and ensuring reliable operation under varying load conditions. A biasing network based on current mirrors is used to generate the required bias currents for all transistors in the circuit, ensuring that they operate in the saturation region for maximum gain and linearity. The op-amp plays a critical role in the DAC by acting as a current-to-voltage converter, maintaining a virtual ground at the output node of the R–2R ladder and converting the ladder current into a proportional output voltage. This configuration improves linearity and minimizes loading effects on the ladder network. The biasing network also enhances the robustness of the design by maintaining consistent operating conditions across process, voltage, and temperature variations.

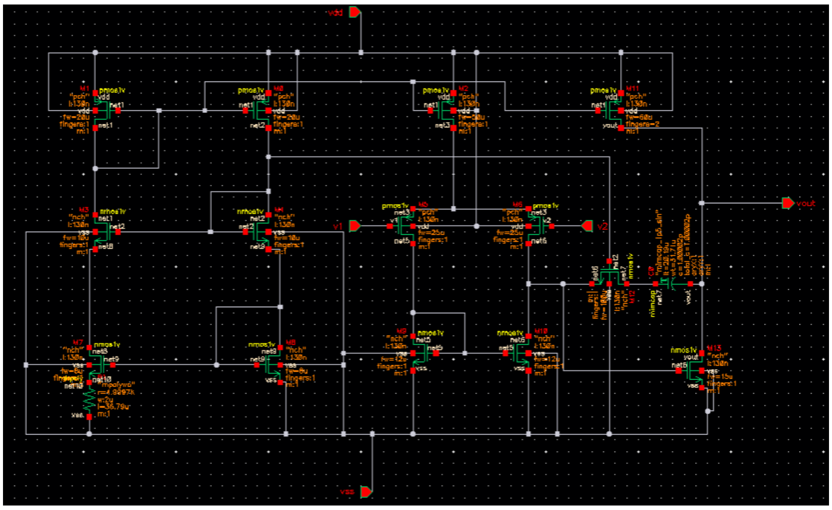

Fig 1. Opamp Schematic

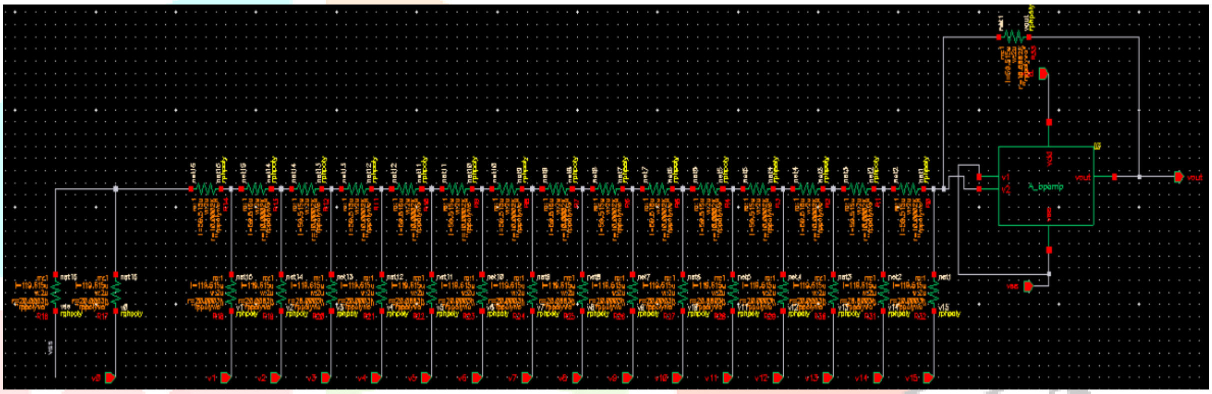

Fig 2. R-2R Ladder

V. RESULTS

The design is simulated using Cadence Virtuoso.

A. *Operational Amplifier Gain*

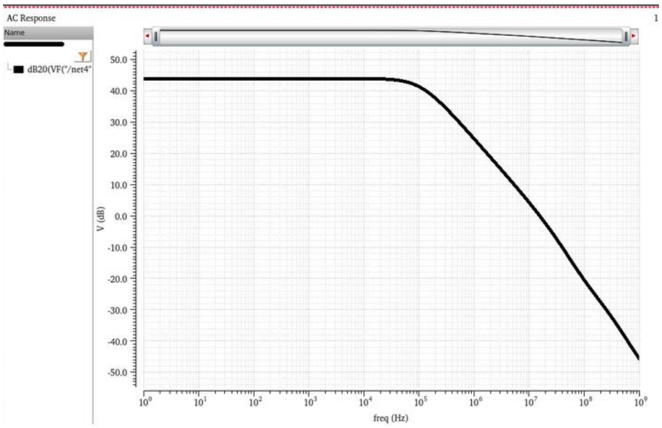

Fig 3. Frequency response of the operational amplifier showing a gain of approximately 42 dB

The open-loop gain of approximately 42 dB is sufficient for basic DAC operation; however, for high-resolution applications such as 16-bit conversion, higher gain is desirable to minimize gain error and improve linearity.

B. *Transient Analysis*

A DAC staircase consisting of 65536 discrete levels is observed, corresponding to the full-scale range of a 16-bit digital input. Each step represents a change of one Least Significant Bit (LSB), indicating that the DAC is capable of resolving very fine voltage differences. The uniform spacing of these steps demonstrates the correct operation of the R–2R ladder network and confirms proper binary weighting of the input bits. As the digital input increases sequentially, the output voltage follows a monotonic rising staircase, which is an essential characteristic of a well-functioning DAC. Due to the high resolution, individual steps are extremely small and may not be visually distinguishable unless zoomed in, effectively making the output appear almost continuous. Minor deviations from ideal step uniformity may be present due to non-idealities such as finite op-amp gain, resistor mismatch, and parasitic effects. Additionally, small glitches may occur during code transitions, particularly when multiple bits switch simultaneously. Despite these practical limitations, the observed staircase behavior validates the successful implementation of a 16-bit DAC and demonstrates its ability to produce high-resolution analog outputs.

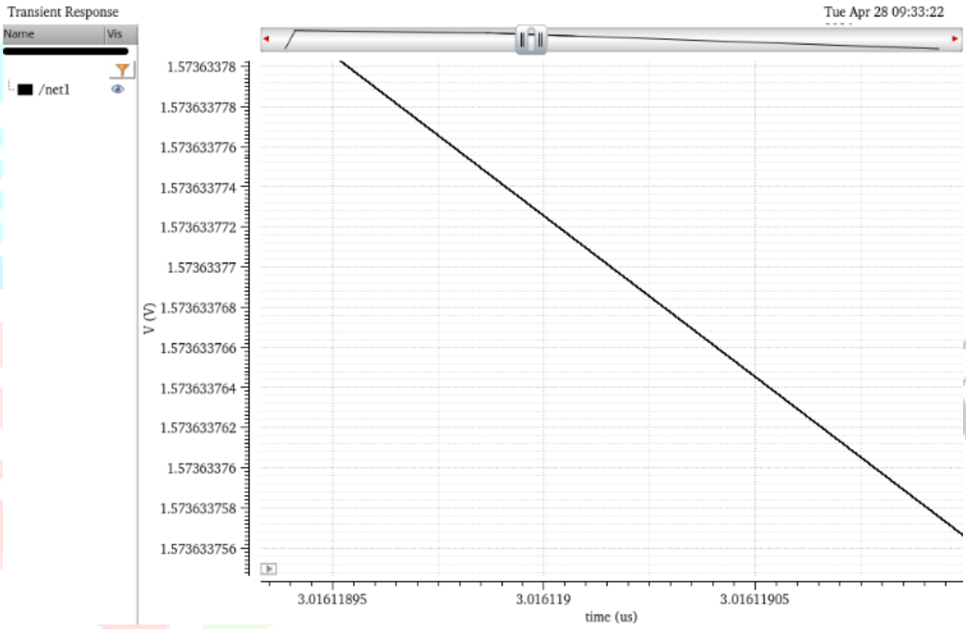

Fig 4. DAC Staircase

VI. CONCLUSION

A 16-bit R–2R DAC has been successfully designed and simulated in 130nm CMOS technology. The results demonstrate correct functionality while highlighting practical challenges in achieving high precision. As seen from the results, the operational amplifier has a gain of 42 dB and operates at a bias current of approximately 20 uA. The DAC staircase shows 65536 levels, which is the full-scale range (2 16 levels). The reference voltage is assumed to be in the range of 1 V to 1.8 V, resulting in a theoretical least significant bit (LSB) step size on the order of 15 uV to 30 uV.

FUTURE WORK

Future work for the R–2R ladder DAC can focus on improving its performance limitations, particularly in terms of linearity, noise, and scalability. One important direction is the use of calibration techniques and digital error correction to reduce INL and DNL errors caused by resistor mismatch. Advanced layout strategies such as common-centroid and interdigitated structures can also be explored to enhance matching in CMOS implementations. Additionally, incorporating segmented architectures (combining R–2R with thermometer coding) can help reduce glitch energy and improve dynamic performance for higher-resolution DACs. Power efficiency can be further optimized by designing low-power switching networks and integrating efficient op-amps or buffer stages. Another promising area is adapting the DAC for ultra-low voltage or highspeed applications, depending on the target use case, as well as exploring process scaling (e.g., 65 nm or below) for better integration in modern systems. Finally, integrating the DAC into a complete mixed-signal system (such as SAR ADC loops or communication systems) and validating it through post-layout simulations and silicon implementation would provide more practical insights and performance validation

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