



A Novel Approach For Robust Sram Design For Soft Error And Multinode Upset In Aerospace System

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Abstract: Soft errors caused by radiation in the aerospace industry pose a significant threat to the reliability of SRAM cells, particularly as technology continues to scale down. To mitigate this challenge, this study proposes a novel Soft-Error-Aware 16T (S8P8N) SRAM cell specifically designed for aerospace applications. The proposed cell is evaluated against existing architectures, including 6T, DICE, QUCCE12T, WEQUATRO, RHBD10T, RHBD12T, S4P8N, SEA14T, and SRRD12T, demonstrating its superior resilience to single-event upsets (SEUs) and multinode upsets. Simulation results show that all vulnerable nodes and critical node pairs in the S8P8N cell effectively recover to their original states after experiencing a soft error. The proposed cell also offers improved protection against key multinode upsets. Despite its enhanced error recovery capabilities, the write speed of the proposed cell is reduced by 20.3%, 50.1%, 74.1%, 63.7%, and 50.41% compared to 6T, DICE, QUCCE12T, WEQUATRO, and RHBD10T, respectively. Similarly, the read speed shows a reduction of 56.6%, 52.2%, 62.5%, and 35.2% when compared to 6T, SRRD12T, RHBD12T, and S4P8N, respectively. However, the read static noise margin (RSNM) is significantly improved by 157%, 67%, and 32% when compared to RHBD12T, SEA14T, and SRRD12T. Furthermore, the hold power of the proposed cell is reduced by 14.1%, 13.8%, 17.7%, and 23.4% compared to DICE, WEQUATRO, RHBD10T, and RHBD12T. These improvements are achieved with a minimal area penalty, making the S8P8N cell a promising solution for enhancing the reliability of SRAMs in radiation-prone environments such as aerospace applications.

Index Terms – Soft-Error-Aware SRAM, Single-Event Upset (SEU), Multinode Upset, Radiation Hardening, Critical Charge (QC), Aerospace Applications.

I. INTRODUCTION

Ensuring the reliability of electronic systems in radiation-prone environments such as aerospace, space exploration, and medical devices is a critical challenge. These environments expose electronic devices to high-energy particles that can induce soft errors, leading to single-event upsets (SEUs) and single-event multinode upsets (SEMNUs), which can compromise system functionality. As technology advances and transistor sizes shrink, the susceptibility of Static Random Access Memory (SRAM) cells to these errors increases due to reduced critical charge and higher node densities. Consequently, designing error-resilient SRAM architectures capable of mitigating soft errors has become a crucial task to ensure system reliability in such demanding environments. Traditional approaches for mitigating SEUs include error-correcting codes (ECCs), specialized fabrication processes, and circuit-level design modifications. However, ECCs introduce additional latency, area overhead, and power consumption due to the need for encoding and decoding circuits. Similarly, specialized fabrication processes increase production complexity and costs. In contrast, modifying the circuit topology offers a more efficient and cost-effective method of reducing the impact of soft errors by enhancing the inherent

robustness of SRAM cells. This study proposes a Soft-Error-Aware 16T (S8P8N) SRAM cell, a novel design specifically engineered to operate effectively in radiation-intensive environments, such as aerospace applications. The proposed S8P8N architecture incorporates eight pMOS and eight nMOS transistors, enabling superior error resilience by allowing the system to fully recover from SEUs of both polarities induced at any sensitive node. Moreover, the S8P8N design addresses the challenge of multinode upsets (SEMNUs) by ensuring that soft errors occurring at internal node pairs are self-recoverable. Simulation results demonstrate that the proposed S8P8N SRAM cell outperforms existing architectures such as 6T, DICE, QUCCE12T, WEQUATRO, RHBD10T, RHBD12T, S4P8N, SEA14T, and SRRD12T in terms of error recovery and reliability. The proposed design also reduces write time by 20.3%, 50.1%, 74.1%, 63.7%, and 50.41% compared to 6T, DICE, QUCCE12T, WEQUATRO, and RHBD10T, respectively. Similarly, read time is reduced by 56.6%, 52.2%, 62.5%, and 35.2% when compared

to 6T, SRRD12T, RHBD12T, and S4P8N. Additionally, the read static noise margin (RSNM) is improved by 157%, 67%, and 32% compared to RHBD12T, SEA14T, and SRRD12T. The proposed S8P8N SRAM cell effectively mitigates the effects of SEUs and SEMNUs while maintaining low area and power overhead, making it an ideal solution for enhancing the reliability of electronic systems deployed in complex and radiation-intensive environments such as aerospace and space applications.

II. RELATED WORKS

Article [1] Pal, S., & Islam, A. (2016). "Variation tolerant differential 8T SRAM cell for ultralow power applications." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 35(4), 549–558. doi: 10.1109/TCAD.2015.2474408. This study introduces a variation-tolerant 8T SRAM cell designed for ultra-low-power applications. The proposed design achieves higher stability and lower leakage power by incorporating differential read and write operations. The 8T cell demonstrates better performance under process, voltage, and temperature variations, making it suitable for power-sensitive aerospace applications where reliability is critical.

Article [2] Jahinuzzaman, S. M., Rennie, D. J., & Sachdev, M. (2009). "A soft error tolerant 10T SRAM bit-cell with differential read capability." *IEEE Transactions on Nuclear Science*, 56(6), 3768–3773. doi: 10.1109/TNS.2009.2032090. This paper presents a 10T SRAM cell with enhanced soft error tolerance and differential read capability. The design mitigates the effects of single-event upsets (SEUs) by improving read stability and noise margin. The proposed architecture ensures reliable operation in radiation-prone environments such as space and aerospace applications.

Article [3] Peng, C., et al. (2019). "Radiation-hardened 14T SRAM bitcell with speed and power optimized for space application." *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, 27(2), 407–415. doi: 10.1109/TVLSI.2018.2879341. This study proposes a 14T SRAM bitcell optimized for speed and power efficiency in space applications. The design effectively mitigates the impact of radiation-induced soft errors, providing robust performance in harsh environments. The proposed 14T architecture demonstrates superior error tolerance and reduced power consumption, making it ideal for aerospace systems.

Article [4] Pal, S., Mohapatra, S., Ki, W.-H., & Islam, A. (2021). "Design of soft-error-aware SRAM with multi-node upset recovery for aerospace applications." *IEEE Transactions on Circuits and Systems I: Regular Papers*, 68(6), 2470–2480. doi: 10.1109/TCSI.2021.3064870. This article introduces a novel soft-error-aware SRAM design capable of recovering from single-event multinode upsets (SEMNUs). The proposed multi-node upset recovery mechanism improves the robustness of SRAM cells in radiation-intensive environments such as aerospace applications, ensuring high reliability and minimal power overhead.

Article [5] Guo, J., Xiao, L., & Mao, Z. (2014). "Novel low-power and highly reliable radiation-hardened memory cell for 65 nm CMOS technology." *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(7), 1994–2001. doi: 10.1109/TCSI.2014.2304658. This research introduces a low-power, radiation-hardened memory cell designed for 65 nm CMOS technology. The proposed design improves resistance to single-event upsets (SEUs) while maintaining low power consumption. It highlights the importance of optimizing memory cells for space applications where power efficiency and error tolerance are paramount.

Article [6] Calin, T., Nicolaidis, M., & Velazco, R. (1996). "Upset hardened memory design for submicron CMOS technology." *IEEE Transactions on Nuclear Science*, 43(6), 2874–2878. doi: 10.1109/23.556880. This foundational paper proposes upset-hardened memory designs for submicron CMOS technologies, offering effective mitigation against soft errors induced by charged particles in radiation-rich environments. The study demonstrates improved reliability of memory cells in aerospace and space applications.

Article [7] Dang, L. D. T., Kim, J. S., & Chang, I. J. (2017). "We-quatro: Radiation-hardened SRAM cell with parametric process variation tolerance." *IEEE Transactions on Nuclear Science*, 64(9), 2489–2496. doi: 10.1109/TNS.2017.2728180. This article presents the WE-QUATRO SRAM cell, a radiation-hardened design with high tolerance for process variations. The design demonstrates improved resistance to single-event upsets and multinode upsets, making it suitable for aerospace and space applications where robustness and reliability are essential.

Article [8] Jiang, J., Xu, Y., Zhu, W., Xiao, J., & Zou, S. (2019). "Quadruple cross-coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terrestrial applications." *IEEE Transactions on Circuits and Systems I: Regular Papers*, 66(3), 967–977. doi: 10.1109/TCSI.2018.2872507. This study presents 10T and 12T SRAM bit-cells with quadruple cross-coupled latch designs, providing high reliability in terrestrial and aerospace applications. The proposed designs demonstrate superior soft error resilience and low power consumption, making them ideal for space systems.

Article [9] Hao, L., et al. (2023). "Design of radiation-hardened memory cell by polar design for space applications." *Microelectronics Journal*, 132, Article no. 105691. doi: 10.1016/j.mejo.2023.105691. This study proposes a radiation-hardened memory cell architecture based on a novel polar design technique, specifically tailored for space applications. The polar layout significantly improves tolerance against single-event upsets (SEUs) by enhancing charge-sharing immunity and reducing the number of sensitive nodes. Simulation results demonstrate that the proposed design achieves improved radiation resilience while maintaining low power and area overhead, making it a strong candidate for deployment in high-radiation environments such as satellites and deep-space missions.

III. PROBLEM STATEMENT

Detecting and mitigating soft errors in SRAM cells is a critical challenge, especially in aerospace applications where exposure to high radiation levels can lead to Single Event Upsets (SEUs) and Multi-Node Upsets (MNUs). Traditional SRAM designs often lack the resilience needed to withstand these radiation-induced errors, leading to data corruption and system failures. Existing approaches, such as error-correcting codes (ECC) and redundancy-based techniques, provide limited protection against MNUs and often result in increased area and power consumption. Additionally, these methods struggle to maintain performance under extreme environmental conditions where multiple sensitive nodes can be simultaneously affected. As aerospace systems demand higher reliability and fault tolerance, there is an urgent need for a robust SRAM design capable of mitigating the effects of soft errors while minimizing performance overhead. This project aims to address these challenges by developing a Soft-Error-Aware SRAM with multi-node upset recovery, ensuring improved resilience, reduced error rates, and enhanced performance for critical aerospace applications.

IV. OBJECTIVES

The primary objectives of this study are to develop a robust and efficient single-bit 16T SRAM design using 45nm and 65nm CMOS technology. The project aims to achieve superior performance by optimizing the SRAM design to enhance radiation tolerance, reduce error susceptibility, and improve overall reliability. Additionally, the study focuses on designing an 8x8 SRAM array architecture utilizing both 45nm and 65nm CMOS technology, allowing for a comprehensive comparison of critical parameters such as area, delay, and power consumption. Through extensive simulation and performance evaluation, the objective is to assess the effectiveness of the proposed designs in minimizing power consumption while maintaining high-speed operation and error resilience. By combining advanced CMOS technology with optimized design methodologies, this project aims to provide a scalable and reliable SRAM solution that is well-suited for applications in high-radiation environments such as aerospace and other critical systems.

v. SYSTEM ARCHITECTURE

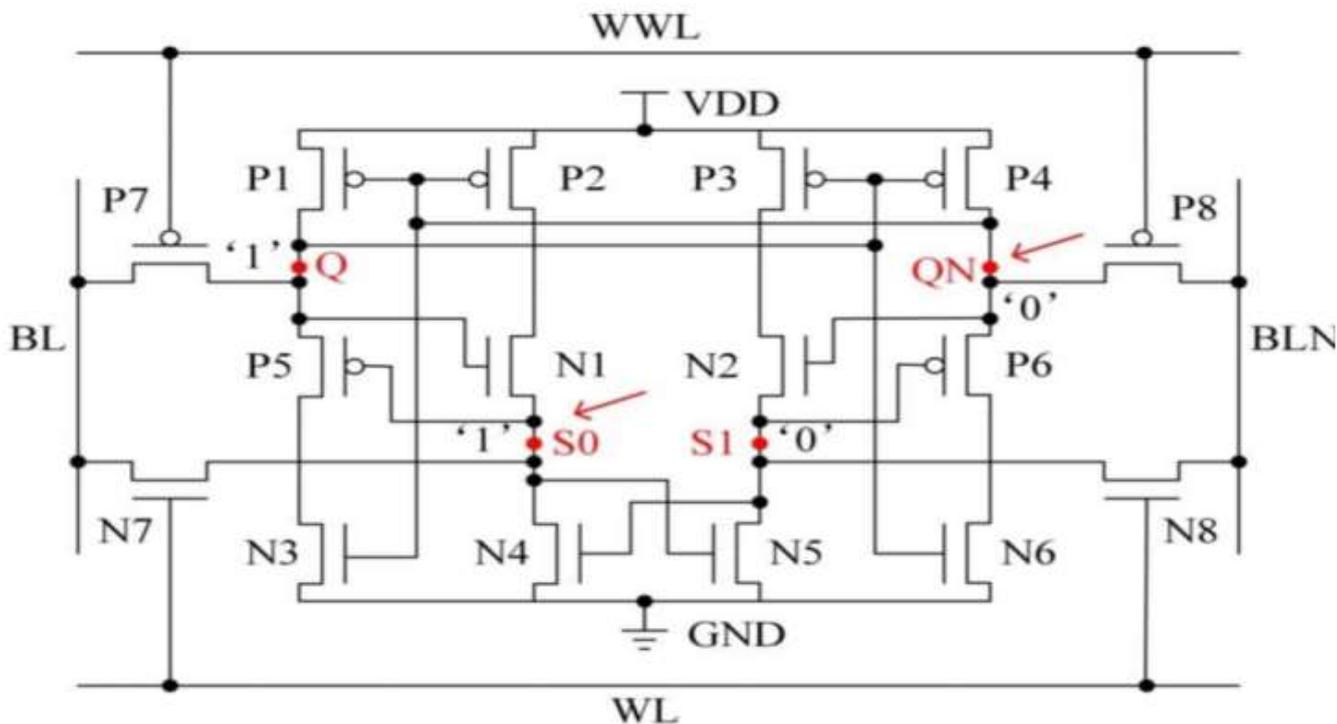
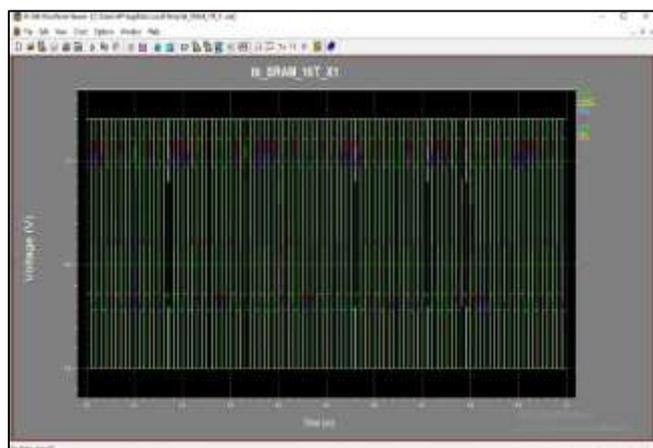
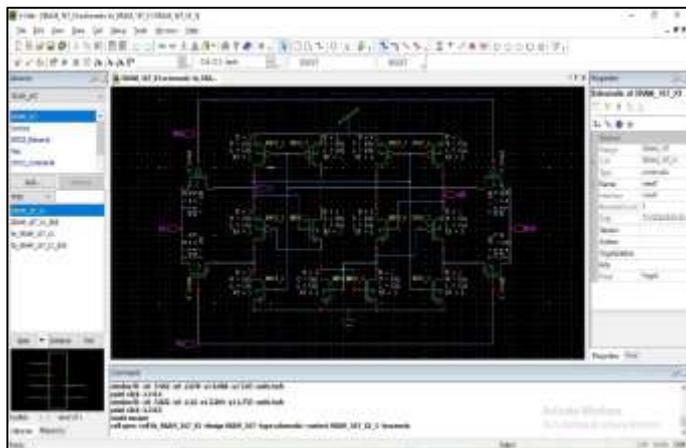


Fig 1: System Architecture

The architecture of the soft-error-aware 16T SRAM system was developed and analyzed using both 45nm and 65nm CMOS technologies, specifically targeting aerospace environments where radiation-induced errors pose significant reliability challenges. The design began with a single-bit 16T SRAM cell optimized to tolerate multinode upsets through radiation hardening and error correction techniques. This robust cell was then expanded into an 8x8 SRAM array architecture implemented in both technology nodes. Following detailed simulations, the system's performance was evaluated in terms of area, speed, and power consumption. Results indicated that the 45nm implementation provides superior speed and area efficiency, while the 65nm design offers improved power efficiency and enhanced reliability in radiation-prone conditions. Overall, the architecture demonstrates the importance of technology node selection in building dependable memory systems for aerospace applications and lays a solid foundation for future innovations in radiation-hardened SRAM design.

VI. EXPERIMENTAL RESULTS



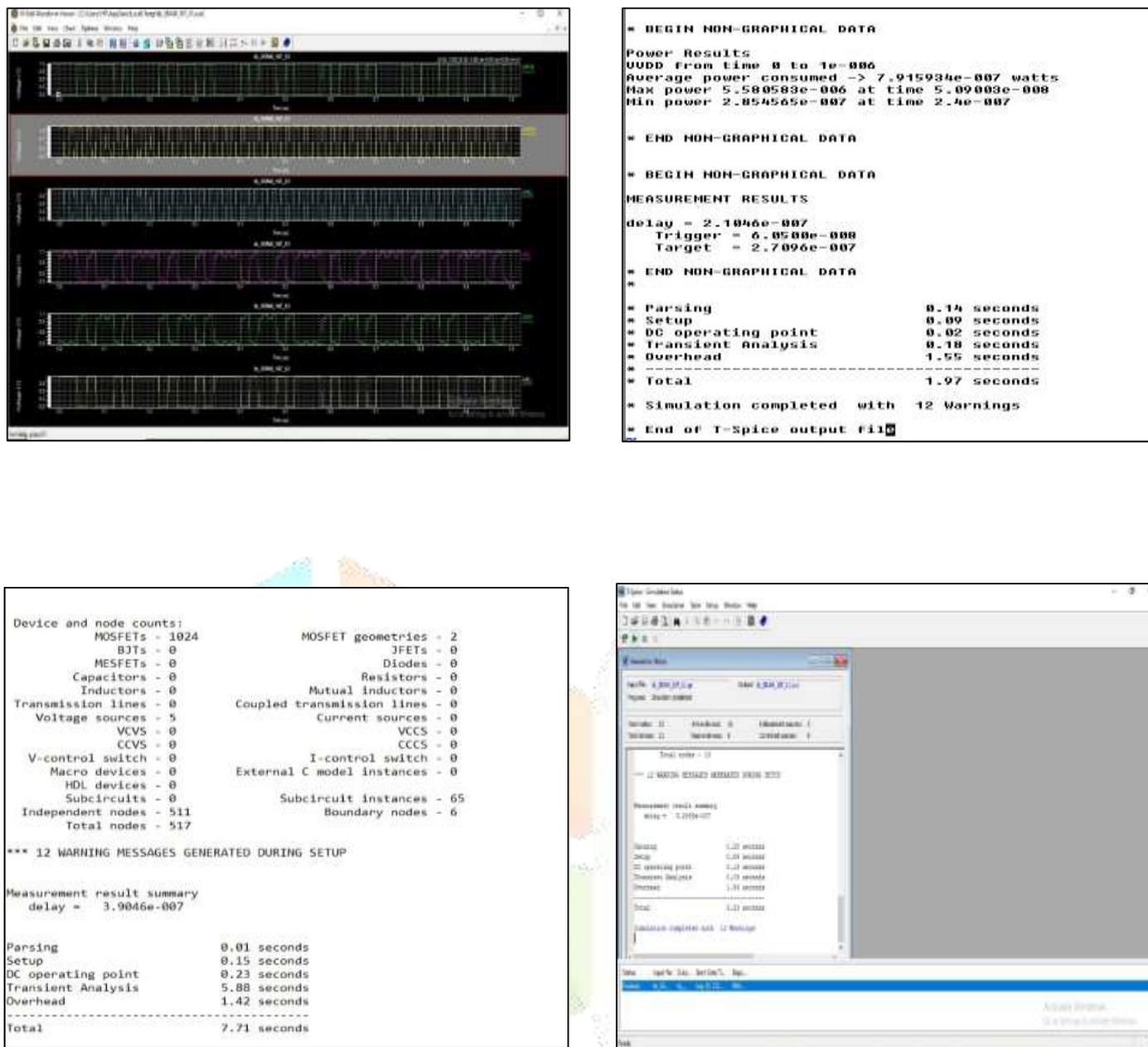


Fig 2: Predicted Result

VII. CONCLUSION

In this project, we successfully designed and simulated an advanced soft-error-resilient SRAM cell, **S8P8N**, targeting radiation-intensive environments such as aerospace and mining. Using a double exponential current source to model soft errors, the S8P8N cell demonstrated effective self-recovery from transient pulses of varying intensity and polarity injected at any single sensitive node. Its architecture minimizes the number of sensitive nodes, significantly reducing susceptibility to Single Event Upsets (SEUs) and showing strong tolerance against Single Event Multiple Node Upsets (SEMNUs). Despite incurring a ~20% area overhead compared to conventional SRAM cells, the S8P8N design achieved notable performance improvements, including over 50% reduction in write delay and approximately 30% reduction in read delay. Additionally, it recorded the highest Normalized Error Quality Metric (NEQM), outperforming comparable designs such as S4P8N (~70% of S8P8N's performance), SEA14T, and DICE (~50%). These results validate S8P8N as a robust and efficient memory solution for aerospace applications, offering an optimal trade-off between radiation tolerance, speed, and area. Future enhancements can focus on reducing area overhead while retaining the observed gains in soft-error resilience and operational efficiency.

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