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Design And Implementation Of Mixed Signal Measurement System Using Fpga

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Abstract: This project presents the design and implementation of a measurement system using a Field-Programmable Gate Array (FPGA) and an Analog-to-Digital Converter (ADC) to process mixed-signal inputs and perform a variety of signal measurements. The system is capable of accurately measuring essential parameters of the input signal, such as voltage levels, 8 bit parallel digital data and 8 bit serial digital data (in formats like hexa decimal or Binary).The FPGA is responsible for the real time processing of the signals and the extraction of these measurements, leveraging its parallel processing capabilities to ensure high-speed performance. The system integrates a USB-to-UART interface for communication between the FPGA and a personal computer. This interface enables the transmission of the measured data to the PC, where it can be displayed and analyzed via a user friendly graphical interface. The measured values, including voltage, digital input are presented on the PC in an easily interpretable format, allowing for real-time monitoring and evaluation of the input signal.

Index Terms - Mixed-signal measurement system, FPGA, ADC, UART, real-time monitoring, signal analysis, digital data acquisition.

I. INTRODUCTION

Measurement system plays crucial role in scientific research, engineering, industrial processes and everyday applications. These systems are designed to observe, analyze, and quantify physical or electrical parameters such as voltage, current, temperature, pressure, frequency, and time. At their core measurement systems bridge the gap between the physical world and digital analysis by converting real-world signals into interpretable data. Modern measurement systems often consist of sensors or transducers, signal conditioning circuits, data converters (e.g., ADCs), processing units, and output interfaces. With advancements in technology, these systems are now equipped with higher accuracy, better resolution, faster processing, and greater flexibility. Measurement systems are widely used in areas such as electronics testing, biomedical instrumentation, industrial automation, and communication networks, making the min dispensable in ensuring product quality system reliability, and operational efficiency.

This project involves the design and implementation of an FPGA-based measurement system integrated with an ADC to analyze mixed signals. The system can measure essential parameters such as voltage levels and data in binary or hexadecimal formats. The FPGA, acting as the core processing unit, enables real-time analysis, high-speed data processing, and adaptability to various signal types. The ADC digitizes the analog components of the input signal, ensuring accuracy during measurement. The extracted data is transmitted to a PC via a USB-to-UART interface, allowing for a user-friendly display and analysis of the measured parameters. This project leverages the reprogrammable nature of FPGAs and the precision of ADCs to provide a versatile and scalable solution for signal measurement challenges. It is well-suited for applications in industries such as electronics, telecommunications, and automation, where precise signal analysis is critical. Few of the uses of our proposed project is that Engineers can use this system to analyze and debug circuits by measuring signal characteristics like voltage levels and frequencies accurately, Real-time

monitoring of signal outputs from machines can ensure operational efficiency and timely maintenance, In education system the system can be used as a teaching and research tool to demonstrate and study signal measurement techniques and FPGA-based designs, In communication system the project can monitor and validate signals in communication devices, ensuring proper functioning and signal integrity, In healthcare system adapted versions can measure and analyze bio-signals like ECG or EEG for diagnostic purposes. Future scope of the proposed project is the system can be upgraded to include advanced signal processing capabilities, such as spectrum analysis, edge detection, or noise filtering, Future versions can support the simultaneous measurement of multiple input signals, making it suitable for more complex systems by incorporating IoT capabilities, the system can transmit measured data to cloud platforms for remote monitoring and predictive maintenance. Integrating AI algorithms can enable the system to detect anomalies, classify signals, or predict potential faults in real-time.

II. LITERATURE SURVEY

In this section, various previous works related to measurement devices and FPGA-based data acquisition systems are discussed. **[1]** N. Corna, F. Garzetti, N. Lusardi, and A. Geraci (2021) proposed a compact, portable, and fully programmable digital instrument for time measurements based entirely on FPGA technology. The device matches the performance levels of the latest ASIC-based Time-to-Digital Converters (TDCs) while offering a low-cost and low-effort solution. It is ideal for applications such as detector testing and time correlation measurements, and it supports rapid prototyping needs. The instrument's features can be easily accessed through a user- friendly Graphical User Interface (GUI) or directly via a software Application Programming Interface (API), providing flexibility and ease of integration into various systems.

[2] Yongfu Xiao, Hao Zhang, and Hao Zou (2020) proposed a quad-channel analog data acquisition system based on FPGA to meet the demands of imaging systems requiring multi-channel input, high resolution, and compact design. The system utilizes a 12-bit ADC (AD9228-65) along with signal conditioning circuits for front-end processing. An FPGA is employed for data acquisition, logic control, and real-time processing. The developed system demonstrates advantages such as low power consumption, reduced cost, high-speed operation, and compact form factor, making it suitable for modern embedded data acquisition applications.

[3] W. Han, Y. Hu, M. Shi, X. Lin, and P. Zou (2024) proposed a high-precision data acquisition system based on FPGA for precision measurement applications. The system integrates an FPGA as the control core, utilizing a multi-gain inverting amplifier with gain settings of ×1, ×10, ×100, and ×1000, implemented using operational amplifiers and analog switches. A 24-bit ADC (AD7175-2) is used for high-resolution signal quantization. Additionally, the FPGA implements FIR low-pass and moving average filters along with error calibration techniques to minimize noise and external interference. Test results demonstrate a DC voltage measurement error of less than 0.05%, making the system suitable for precision applications such as optical radiation measurement.

[4] Soyeon Choi, Heehun Yang, Yunjin Noh, Giyoung Kim, Eunsang Kwon, and Hoyoung Yoo (2024) proposed a multi-channel real-time data acquisition system based on FPGA to address limitations in cost and channel scalability of conventional systems like NI USRP-RIO. The proposed system employs a 16-channel ADC capable of up to 100 MSPS and integrates signal acquisition and processing on a single chip using a one-chip architecture. By implementing pipelining techniques, the system enables real-time data processing without inter-device latency. Utilizing the TI ADS52J90 ADC and a Kintex UltraScale KCU105 FPGA board, the design supports simultaneous multi-channel input and efficient processing, making it suitable for applications in acoustics, radar, sonar, and navigation while also reducing system cost and processing time.

[5] G. Dhanabalan and T. Murugan (2021) proposed an FPGA-based Successive Approximation Register (SAR) type ADC analog input module (AIM) for industrial applications, aiming to improve the efficiency of data acquisition in programmable logic controller (PLC) systems. The design integrates a DAC, comparator, and FPGA to implement a single-channel ADC, and scales to multi-channel acquisition by replicating these components. Unlike traditional processor-based AIMs, where the total conversion time scales with the number of channels (n × tc), the FPGA-based approach achieves concurrent processing, maintaining a fixed conversion time (tc) regardless of channel count. Experimental results using Multisim demonstrated a conversion time of 0.13 ms for eight channels, indicating significant performance improvements suitable for real-time industrial environments.

[6] Anchal Govil, Anmol Karnwal, Govinda Sindhu, Ayush Singh, and Shubham Shukla (2022) proposed a UART (Universal Asynchronous Receiver-Transmitter) controller implemented on an FPGA using a microprogrammed control architecture. The design, developed in Verilog and synthesized on a Spartan-3E FPGA using Xilinx ISE Webpack 14.7, demonstrated a maximum operational clock frequency of 218.248 MHz, with the UART controller operating reliably up to 192.773 MHz. The implementation is efficient in resource usage and fully functional, highlighting the advantages of high-speed communication and compact design for embedded applications.

[7] Changqing Yang, Dawei Zhou, and Li Lu (2022) proposed a multi-channel high-speed data acquisition system based on improved SPI communication to enable synchronized acquisition of voltage and current parameters across master and slave FPGA control boards. Developed using the Vivado platform, the system enhances traditional SPI by increasing the number of MISO lines, significantly boosting the data transfer rate and effectively utilizing FPGA I/O resources. A data conversion module is integrated for intuitive observation of results. The system demonstrates high-speed acquisition with high measurement accuracy within the designated voltage input range, confirming its suitability for real-time multi-channel data monitoring applications.

III. RESEARCH METHODOLOGY

Block diagram:

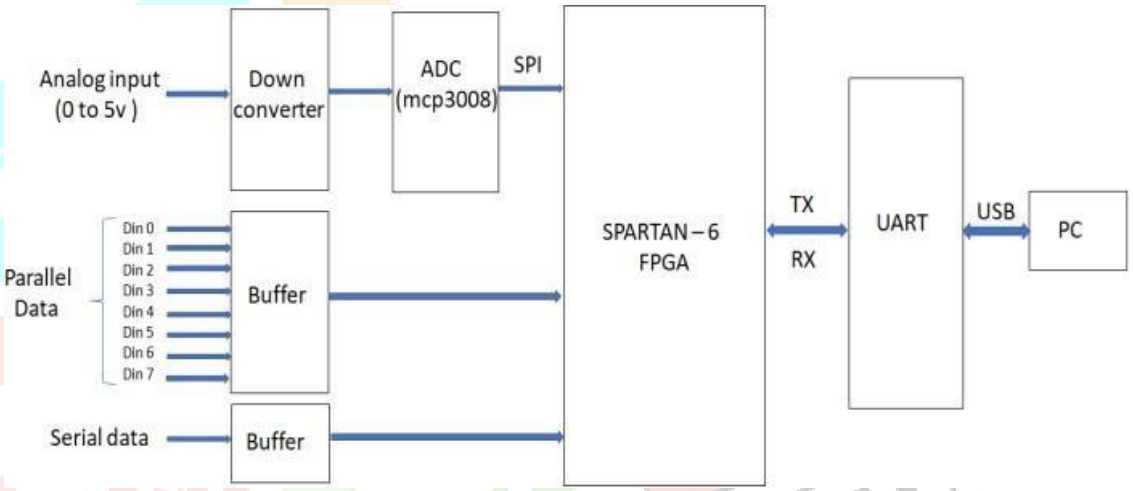


Figure-1:Block Diagram of signal measurement system

The methodology of this project revolves around the implementation of transmitter and receiver modules to enable communication through a terminal interface. The system responds to user inputs to perform specific tasks. When the user presses the "I" key, the transmitter sends a predefined message to the terminal, confirming successful communication. If theuser presses "R", the system captures 8-bit parallel data from eight designated input pins simultaneously and then transmits this collected data back to the terminal for display. Alternatively, when the user presses "r", the system captures 8-bit serial data from a single input pin, bit by bit, before transmitting the complete byte to the terminal. This structured approach ensures flexible and interactive data handling, demonstrating the functionality of both parallel and serial data acquisition using the developed UART communication modules.

The system uses a Universal Asynchronous Receiver Transmitter (UART) protocol for serial communication between devices. This protocol operates using just two signal lines: one for transmitting (TX) and the other for receiving (RX). Data is transmitted asynchronously in a frame-based format, which allows two devices to communicate without a shared clock signal. Each UART frame consists of a start bit, followed by data bits, an optional parity bit, and a stop bit. The line remains high during idle states. A start bit represented by a low signal—indicates the beginning of a transmission. Once the data has been sent, a stop bit represented by a high signal marks the end of the frame. This structure enables consistent and efficient communication, even over simple hardware setups.

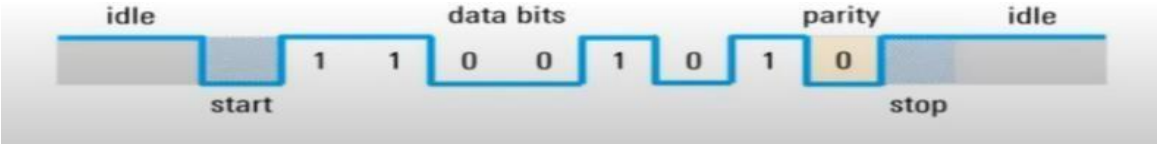


Figure-2: UART

Since UART operates asynchronously, the transmitter and receiver do not share a common clock signal. Instead, both devices must be configured to transmit and receive data at the same predefined speed to ensure proper communication. This characteristic eliminates the need for clock synchronization lines, simplifying hardware design while maintaining reliable data exchange. In the proposed FPGA-based signal measurement system, the UART interface has been configured to operate at a baud rate of 115200 bits per second, balancing ease of implementation with sufficient data throughput for real-time signal control and monitoring.

Common UART baud rates
4800
9600
19200
57600
115200

Figure-3:Baud rate

The transmitter and receiver in the proposed FPGA-based signal measurement system are modeled using finite state machines to ensure accurate UART communication. The UART transmitter operates through a sequence of states: Idle, Start, Transmit, and Stop. In the Idle state, the system continuously monitors the RX line, waiting for a specific input character, such as "R", "r", or "l", to initiate communication. Once a valid character is received, the transmitter moves to the Start state, where the start bit is transmitted by setting the TX line low (TX = 0) at the predefined baud rate. Following the start bit, the system transitions to the Transmit state, where each data bit is sequentially sent over the TX line, also adhering to the known baud rate. After transmitting all eight bits of the data frame, the system proceeds to the Stop state, where a stop bit is transmitted by setting the TX line high (TX = 1). Upon completion of the stop bit transmission the transmitter returns to the Idle state, ready to handle the next incoming data frame.

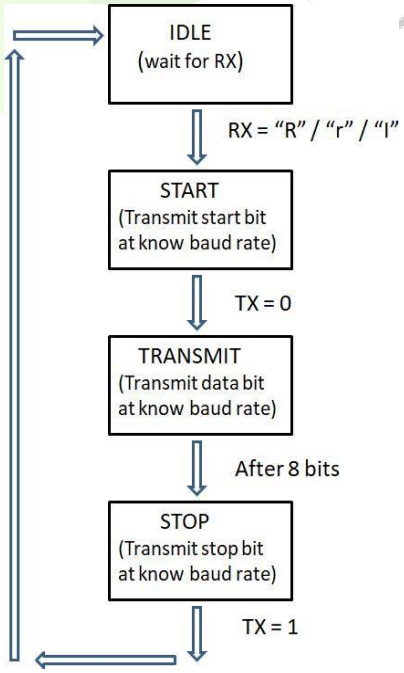


Figure-4:State diagram of transmitter

The UART receiver operates through three primary states: Idle, Receiving, and Validate. In the Idle state, the system continuously monitors the RX line, waiting for the detection of a start bit indicated when RX goes low (RX ='0'). Upon detecting the start bit, the receiver transitions to the Receiving state, where it begins sampling incoming bits at the predefined baud rate. It collects a total of 10 bits, which include the start bit, eight data bits, and the stop bit. After all 10 bits have been received, the system moves to the Validate state, where it checks the correctness of the stop bit to ensure the integrity of the received data. If validation is successful, the receiver outputs the captured data and returns to the Idle state, ready for the next incoming transmission.

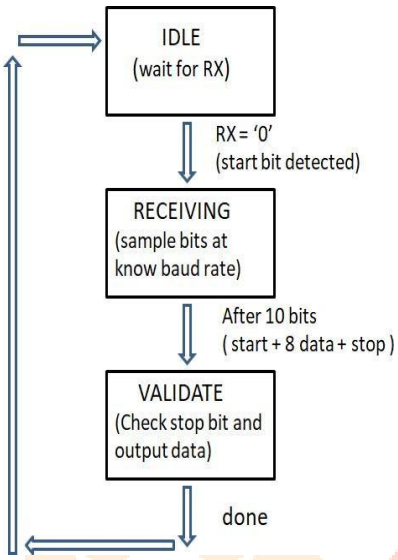
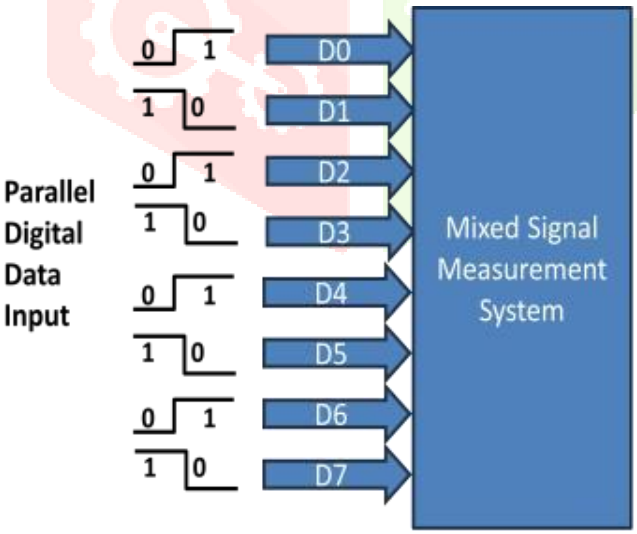


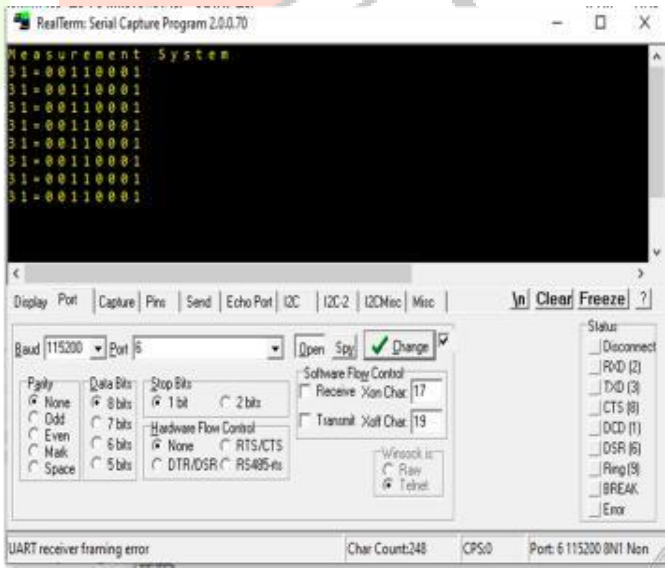
Figure-5:State diagram of receiver

IV. RESULTS

8-Bit Parallel Digital Data:

1) Input Data: 0x31
   For input Data 0x31the binary Value is “00110001”

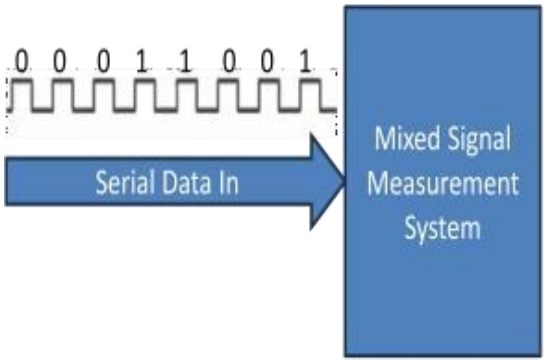


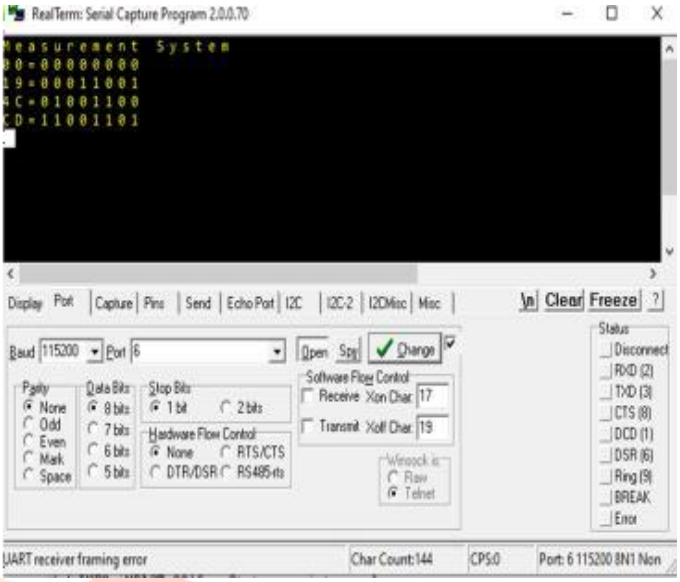


8-Bit Serial Digital Data:

2) Input Data: 0x19

For input Data 0x19 the binary Value is “00011001”





V. CONCLUSION

The digital section of the proposed mixed-signal measurement system has been successfully implemented and verified. It supports both parallel 8-bit input and serial UART input, enabling real-time acquisition of digital data. The system accurately converts the incoming data into hexadecimal, binary, and ASCII formats, and transmits the processed information to a PC terminal via a USB-to-UART interface. This achievement demonstrates the system’s capability to handle various digital formats efficiently using the FPGA’s parallel processing power. The UART module ensures smooth and reliable communication, making the system user-friendly and adaptable for debugging and embedded system testing.

VI. FUTURE SCOPE

The successful completion of the digital part lays a strong foundation for the integration of the analog section, where the FPGA will interface with an ADC using the SPI protocol to complete the mixed-signal measurement system.

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