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A Comparative Study of Different Topologies of Multilevel Inverter to Reduced Total Harmonic Distortion (THD) and Increase the Output Voltage

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Abstract – This paper introduces an investigation of PWM techniques which can minimize total harmonic distortion (THD) and enhance the output voltage. Also this paper present a comparison between different topologies of multilevel inverter. This comparison is done with respect of weight, THD and cost. For multilevel inverters IGBT's and MOSFET's are used as switching devices to make the inverter more accurate. Multilevel inverters are important for power electronics application such as, active power filters and uninterruptible power supplies. If THD is important, the 11 level inverter should be used, since it has lower THD than 9 level and 5 level inverter. If cost is important 5 level inverter be used. If power losses are important the 9 level diode clamped inverter is used. To select a multilevel inverter is tradeoff between cost, complexity, losses and THD. The most important part is to decide which one is important.

Key words: multilevel inverters, pulse width modulation, total harmonic distortion, power losses and Loss.

Introduction

This paper compares three different topologies of inverters (one level inverter, Diode clamped inverter, Flying capacitor clamped inverter and switching devices to make the comparisons more accurate. The switches that are used for different inverters are the same for all of the inverters. inverters are 5-level and 9-level inverters. This comparison is done with respect of power losses, cost, weight and THD. The switching pattern for (There is no control on inverter; also for loss calculation loading distribution is assumed.) Cascaded H-bridge inverter). The multilevel inverters is explained as well. These inverters are connected to a 400V, 75kW asynchronous motor. For each inverter, IGBTs and MOSFETs are used as

If the THD is important, the 9-level inverters should be used, since it has a lower THD than the 5-level and the two-level inverter. The 9-level multilevel inverters have the lowest THD when filters are not used. Their THD is about 7%. If the cost is important the two-level inverter should be used, since it has the lowest cost between all of the inverter topologies. If the power losses are important, the 5-level diode clamped is the best choice since it has the lowest power losses between all other inverter topologies. If the weight is important the two-level inverter is the best choice since it has the lowest weight between all other inverter topologies. Its weight is about 5Kg. If the power

losses are important, the 5-level flying capacitor is the best choice, since it has the lower power losses between all the other inverter topologies. To select a multilevel inverter is a tradeoff between cost, complexity, losses and THD. The most important part is to decide which one is more important.

Multilevel inverters

Three types of multilevel inverter have been investigated in this paper.

1. Diode Clamped multilevel inverters
2. Flying Capacitor multilevel inverters
3. Cascaded H-bridge multilevel inverters

2.1. Diode Clamped multilevel inverter

The main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is V_{dc}. An *n* level inverter needs (*n*-1) voltage sources, 2(*n*-1) switching devices and (*n*-1) (*n*-2) diodes. 5-level diode clamped multilevel inverter

2.1.1 5-Level diode clamped multilevel inverter

A 5-level diode clamped multilevel inverter is shown in Fig. 1. Switching states are shown in Table.1. For example to have $V_{dc}/2$ in the output, switches S_1 to S4 should conduct at the same time. For each voltage level four switches should conduct. As it can be seen in Table.1 the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using a two times voltage source or cascading two diode clamped multilevel inverters. The output voltage of a 5-level diode clamped multilevel inverter is shown in Fig.1. As can be seen in Fig.1 all of the voltage level should have the same voltage value.

The switching angles should be calculated in such a way that the THD of the output voltage becomes as low as possible. The switching angle calculation method that is used in this paper is the harmonic elimination method. In this method the lower dominant harmonics can be eliminated by choosing calculated switching angles. This method will be explained later in this paper.

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_{dc}/	1	1	1	1	0	0	0	0
V_{dc}/	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-V_{dc}	0	0	0	1	1	1	1	0
-V_{dc}	0	0	0	0	1	1	1	1

Table 1. The switching states of Diode clamped multilevel inverter.

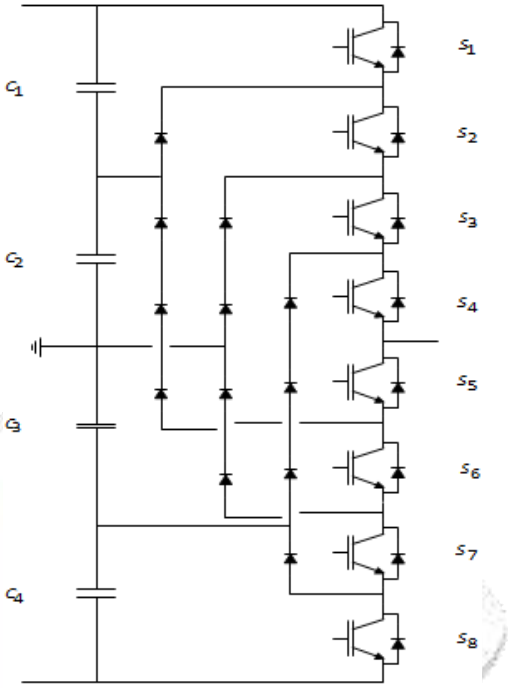


Figure 1. One phase of a diode clamped inverter

Flying capacitor multilevel inverters

This inverter uses capacitors to limit the voltage of the power devices. The configuration of the flying capacitor multilevel inverter is like a diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is V_{dc}.

2.2.1. 5-level flying capacitor multilevel inverters

For a 5-level flying capacitor multilevel inverter:

n=5

Therefore:

Number of switches=8

Number of capacitor

s= 10

Fig. 2 shows a five level flying capacitor multilevel inverter. The switching states in this inverter are like in the diode clamped multilevel inverter. It means that for each output voltage level 4 switches should be on. Table.2 shows the switching states for a 5-level flying capacitor clamped multilevel inverter. The output voltage was shown before in Fig.1.

The switching angles like the diode clamped multilevel inverter should be calculated in such a way that the THD of the output voltage becomes as low as possible. The method is the same as the diode clamped inverter.

V_0	S	S	S	S	S	S	S	S_8
V_{dc}/	1	1	1	1	0	0	0	0
V_{dc}/	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
-V_{dc}	1	0	0	0	1	1	1	0
-V_{dc}	0	0	0	0	1	1	1	1

Table 2. The switching pattern for capacitor clamped multilevel inverter.

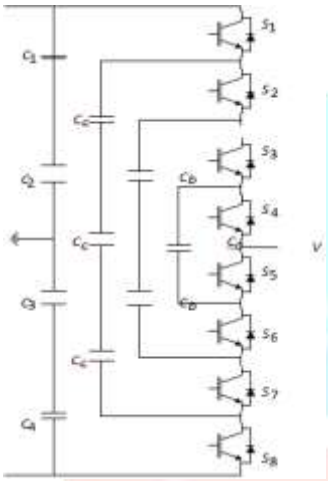


Figure 2. One phase of a 5-level Flying capacitor multilevel inverter

Harmonic elimination method

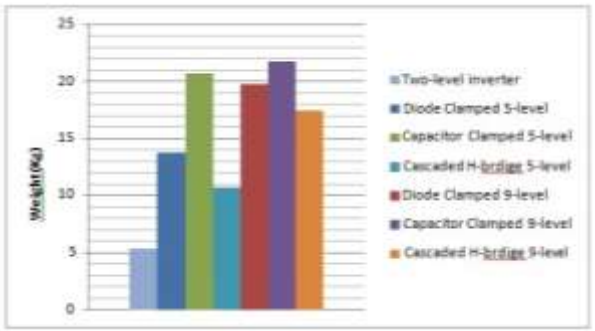
The switching pattern that is used in this paper for all of the multilevel inverters is harmonic elimination method. In this method the switching angles for switches should be calculated in such a way that the lower dominant harmonics are eliminated. In this case 5-level and 9-level multilevel inverters will be investigated. For a 5-level inverter the 5^{th} harmonic will be eliminated and for the 9-level inverter the 5^{th}, 7^{th}, 11^{th} harmonics will be eliminated. The Fourier analysis needs to be calculated to determine the frequency spectra of the output waveform.

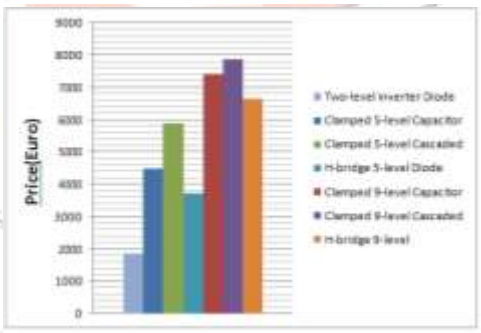
Weight and cost comparisons

Weight comparison is done for each topology by calculating the weight of all of the components of the inverters. The same switch is considered for all of the topologies to have a more accurate comparison. The IGBT FD300R06KE3 is used for all of the topologies. In the

5-level diode clamped multilevel inverter, the 5-level flying capacitor, the 5-level cascaded H-bridge and the two-level inverter, the capacitor C4DEFPQ6380A8TK is used, since the DC input voltages are higher, so a capacitor with higher voltage tolerance is needed. In the 9-level diode clamped multilevel inverter, the 9-level flying capacitor multilevel inverter and the 9-level cascaded H-bridge multilevel inverter the capacitor FFV34E0107K is used, since the DC input voltages are lower, so a capacitor with lower voltage tolerance is needed.

Weight comparison for all topologies of inverters

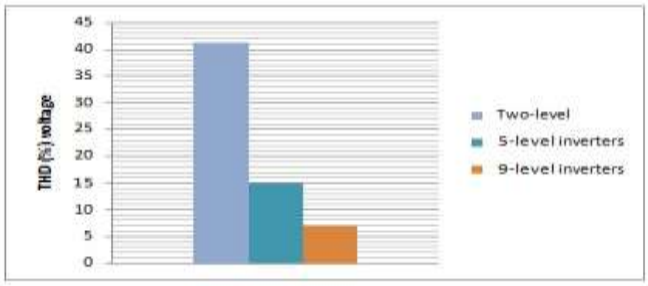




Cost comparison for all topologies of inverter

THD comparison for all of the inverter topologies

THD calculations obtained from the SIMULINK file. All of the THDs are for stator current in the electrical motor. The THD comparison between the 5-level inverters, the 9-level inverters and the two-level inverters is shown in Fig. The output voltage of all the 5-level topologies is the same, since the same switching pattern is used for all of them. The output voltage of all the 9-level inverters is the same, since the same switching pattern is used for all of them.



Voltage THD comparison for all inverter topologies

Conclusions

The choice of topology for each inverter should be based on what is the usage of the inverter. Each topology has some advantages and disadvantages. By increasing the number of levels, the THD will be decreased but on the other hand cost and weight will be increased as well. Also since the switching angles for switches are not the same, the drive circuit for each switch is separate from other switches.

The two-level inverter has the lowest cost and weight in comparison with the other topologies. But this inverter has a very high THD; its THD is about 40% when one switching event for fundamental period is used. In weight and cost calculations, the price and weight of the filter should be considered, since it is not practical to have an output voltage with 40% THD. The cost and the weight of the 5-level multilevel inverters seem better than the 9-level multilevel inverters. By increasing the number of levels, the cost and weight of the multilevel inverter will be increased. The advantage that the 9-level multilevel inverters have over the 5-level multilevel inverters is their THD before filters, thus a filter will be needed. The 9-level multilevel inverters have lower THD than the 5-level multilevel inverters. For example the THD in the 5-level multilevel inverters and the 9-level inverters are 15% and 7%. It seems that using the 5-level inverter and a filter is a better design.

The Flying capacitor clamped inverter has the lowest power losses between all of the other topologies, since there is no diode in its topology. For example the power losses in the 5-level flying capacitor multilevel inverter in full load are 625W, but it has two big problems. First is that it is heavier than the other topologies. It is not practical to use this heavy inverter in applications that are going to be used in applications that are not stable. Also the cost of this inverter is more than other inverters. It seems that the flying capacitor clamped multilevel inverter can be used in applications where the power losses are more important compared to the weight and cost.

The cascaded H-bridge has the lowest weight and cost between the multilevel inverters, but its power losses is more that all the other topologies. For example at compared to the other topologies its power loss is 3749W. This topology can be used in applications where the weight and the cost of the application is more important than its power losses.

The diode clamped multilevel inverter's power losses are lower than cascaded H-bridge. For example the power losses in the 9-level diode clamped multilevel inverter are 2963W. The diodes that were used in this paper cost 6.95 Euros, so the cost will not be that much higher than the cascaded H-bridge. It seems that diode clamped inverter is a topology between all other topologies that THD, cost and power losses are between other types of inverters.

Reference

[1] Muhammad H. Rashid, Power Electronics circuits, devices, and applications. 2004 by Pearson education Inc.

[2] Zhong Du, Leon M. Tolber, Burak Ozpineci, John N. Chiasso, DC-AC Cascaded H- Bridge Multilevel Boost Inverter With No Inductors for Electric/Hybrid Electric Vehicle Applications. 2009, Boise state university

[3] Martin Veenstra, INVESTIGATION AND CONTROL OF A HYBRID ASYMMETRIC MULTI-LEVEL INVERTER FOR MEDIUM-VOLTAGE APPLICATIONS, 2003, Lausanne, EPFL

[4] L.M. Tolbert, F.Z. Peng, D.J. Adams, J.W. Mckeever, Multilevel inverters for large automotive electric drives, 1997, Darborn, Michigan

[5] K.T. Chau, Y.S. Wong, Overview of power management in hybrid electric vehicles, 2002, Energy conversion and management 43

[6] Chris Mi, Fang. Z. Peng, Kenneth J. Kelly, Michael O'Keefe, Vahab Hassani, Topology, design, analysis and thermal management of power electronics for hybrid electric vehicle applications, International journal of Electric and Hybrid vehicles, Vol.1, 2008

[7] Fang Z. Peng, A Generalized Multilevel Inverter Topology with Self Voltage Balancing, IEEE transaction on Industry applications, Vol. 37, 2001

[8] Leon M. Tolbert, John Chiasson, Keith McKenzie, Zhong Du, Elimination of harmonics in a multilevel converter with non equal DC sources, IEEE transaction on Industry applications, Vol.41, 2005

[9] José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng, Multilevel Inverters: A Survey of Topologies, Controls and Applications, IEEE transaction on Industry Electronics, Vol.49,

[10] Leon M. Tolbert, Fang Z. Peng, Multilevel Converters as a Utility Interface for Renewable Energy Systems, Power engineering society summer meeting, 2000, IEEE

[11] Leon M. Tolbert, Fang Zheng Peng, Tim Cunnyngham, John N. Chiasson, Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles, IEEE transactions on industrial electronics, Vol.49, 2002

[12] John N. Chiasson, Leon M. Tolbert, Keith J. McKenzie, Zhong Du, Control of a multilevel inverter using resultant theory, IEEE transaction on control systems technology, Vol.11, 2003

[13] D. Grahame Holmes, Thomas A.Lipo, Pulse width modulation for power converters, 2003 by Wiley interscience Inc.