IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Design of an FPGA based Walsh-coding Scheme for Human Body Communication

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***Abstract*:**

This paper reports the design and implementation details of a transceiver architecture for application in wearable devices deploying human body as the transmission medium. The human body communication (HBC) is a non-Radiofrequency communication defined in the IEEE 802.15.6 standard, exclusively for Wireless Body Area Networks (WBANs). In this design, which is based on Walsh coding scheme, high data rates up to10 Mbps for WBAN applications have been achieved, simultaneously reducing the design complexity and resource utilization by 25.7% in comparison to BCH codes used for ultra-wide band communication. The simulated design has shown a low power utilization of 87mW and employs only 37 slices, when implemented on Artix7 FPGA device.

Index Terms

Human Body Communication (HBC), Wireless Body Area Network (WBAN), non-RF communication, Walsh Codes, HBC transceivers

I. Introduction

Human Body Communication (HBC) is a non-RF communication designed using IEEE 802.15.6 standard for WBAN, finding a range of applications in medical, sports, defense etc. In implementing WBAN's , the intra body communication systems (IBC) that use human body as the communication channel (via capacitive and galvanic coupling) have gained lots of attention in the recent years [1]. In capacitive coupling the ground terminal is left floating, whereas in galvanic coupling the transmitter and receivers are connected to human body. In the reported literature [2-8] the typical modulation techniques chosen are the BPSK, QPSK, MSK and 16 PAM, QPSK for less hardware complexities. BPSK was also used for cases that consider empirical measurements.

The design of transceivers for HBC considers various factors like data rate, power consumption, resource utilization and operating frequency. To improvise the data rate one of the factors is to select an appropriate encoding scheme for modulation. The error correcting codes are used to improvise the performance of the transceiver design. Error correcting codes (ECC) are classified as forward error correcting (FEC) codes and modulation. The design of ECC has numerous challenges like power management and reliability for varying data rate. The proper design of ECC leads to an efficient transceiver in power management, since the process of battery replacement is a difficult process in WBAN applications. In this direction, an extensive survey was carried out in order to arrive at the methodology of this research work.

The carrier frequency and modulation method are selected based on the channel characteristics. PSK is used for low bit rate applications and moderate error performance for capacitive coupling, OOK provided a data rate of 2.4Kbps [1] which was enhanced to 9.6Kbps using FSK.164Kbps and 1.313 Mbps were achieved using delay locked loop based BPSK. Wideband signaling could achieve a data rate of 2Mbps using direct coupled interface (DCI).

In IBC systems, a high carrier frequency is selected to be in the range of 200MHz for low path loss [2] and for a maximum channel gain a low frequency of 10MHz was chosen [3]. Human body behaved as a bandpass filter with bandwidth of 100MHz.[4]. Frequency hopping FSK and DSSS extended data rate up to 10Mbps. A wideband signaling HBC transceiver with high data rate between 1Mbps to 40Mbps was developed by Chung et al [5]. Manchester code could provide a data rate of 10Mbps with power consumption of 22uW [6]. Galvanic coupling, and 0.9Kbps data rate was achieved using PWM.

Using FSK, 9.6 kbps data rate was obtained using a carrier frequency of 10.7 MHz A data rate of 255 kbps and 128 kbps, was obtained using BPSK and FSK respectively [7]. Complexity of hardware was reported to be similar for OOK and PPM. An energy efficient PPM transmitter was designed for galvanic IBC as PPM is time based and is more immune to false detection compared to OOK, which is shape based modulation scheme [8]. A data rate of 1.56Mbps was achieved with a power consumption of 2.0mW. Modifications to WBS was done in terms of encoding scheme where NRZI was used to transmit data [9] which provided a data rate of 40Mbps with a power consumption of 1.94mW

The paper is organized as follows: Section II provides the background of ECC, Section III includes the implementation details of Walsh coder, on which the present work is based, and finally the results and discussion are provided in Section IV.

II. Background

The noisy channels use the FEC codes to detect the error bits and correct the data values. The redundant bits are added to the data values on the sender side which are encoded by the FEC encoder. On the receiver side the FEC decoder detects the error bits by making use of redundant bits and the original data values are retrieved. There are mainly two types of FEC coding schemes available: block codes and convolutional codes [10].

Block codes are fixed size blocks represented as bits, symbols or codewords and memoryless codes. They support hard code decisions. The existing works quote codes like Reed Solomon Coding, Golay codes, LDPC codes, Hamming Codes, and BCH Codes. The convolution codes are represented in terms as bits of stream of varying length and they possess memory. They support soft code decisions. The existing codes in literature are convolution codes, Turbo codes and many more.

The advantages of FEC codes are mainly: simple design implementation, faster implementation based on the algorithm and offer a higher degree of fault tolerance which results in lower BER. FEC codes are suitable for distant communication system. The FEC codes have limitations like not suitable for short range communications and the redundant bit addition incurs more costs. So, FEC codes are not used in HBC and hence led to the formulation of standard modulation technique for a data rate suitable for HBC in IEEE 802.15.6. In this paper, frequency selective digital transmission (FSDT) with Walsh coding is studied for WBAN applications.

III. Methodology

The methodology adopted for Walsh coding is represented in Figure.1. The Frequency Selective (FS) spreading and despreading unit has Walsh codes as one of the components in HBC system. Walsh encoding and decoding unit are part of data generation in transmitter and data recovery in receiver. The operation of Walsh coding is been studied in this paper and the results are promising compared to the other coding schemes reported, to the best of our knowledge.

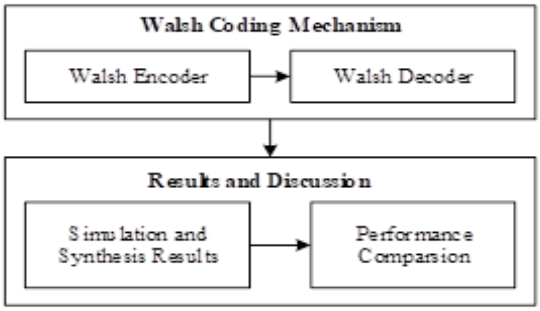

Figure 1: Methodology adopted for the Walsh coding.

IV. Implementation

The orthogonality property of Walsh codes aids in error correction of data transmission in HBC system. The architecture of Walsh coding is represented in Figure 2. The encoder unit comprises of a serial to parallel converter (S2P) and an encoding unit. Similarly, the decoder unit has a decoding unit and a parallel to serial converter(P2S)

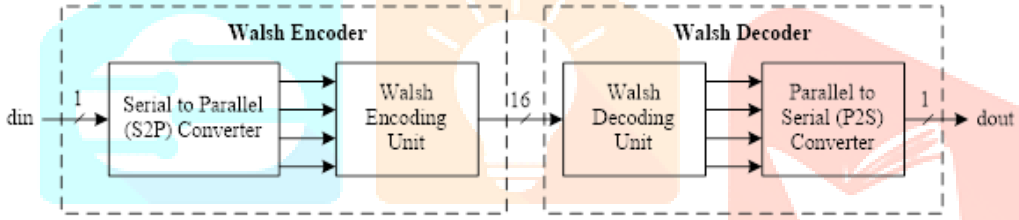

Figure 2: Architecture for the Walsh coding.

The serial data received on din is processed using a S2P converter, which converts into 4-bit parallel output. The implementation of S2P converter is possible with 4 D Flipflops as achieved in a serial to parallel conversion. The output of the S2P converter is provided to the encoding unit where the 4-bit symbol is mapped to its corresponding 16-bit Walsh code as shown in Table1. The output of encoding unit is provided as the input to the decoder unit where the 16-bit Walsh codes are reconverted into 4-bit data. The P2S converter later recovers the 1-bit serial data dout. The Walsh encoder data is multiplied with 8 -bit frequency shift code (FSC) to generate the data output of the transmitter. Similarly, at the receiver the data is divided by FSC to generate the FS-despreader output in an HBC system.

Table.1 Symbol mapping to Walsh codes in S2P

S2P Output bits	Orthogonal Code	S2P Output bits	Orthogonal Code
0000	1111111111111111	1000	1111111100000000
0001	1010101010101010	1001	1010101001010101
0010	1100110011001100	1010	1100110000110011
0011	1001100110011001	1011	1001100101100110
0100	1111000011110000	1100	1111000000001111
0101	1010010110100101	1101	1010010101011010
0110	1100001111000011	1110	1100001100111100
0111	1001011010010110	1111	1001011001101001

V. Results and Discussion

The Walsh coding module is synthesized and implemented on Artix-7 FPGA device. Modelsim 6.5F is used for simulation and verification of the functionality. The obtained results are analyzed based on the design constraints of power consumption, chip area and timing. The obtained results are compared with the existing works. The internal architecture of Walsh encoder and decoder unit is shown in Figure 3 and the simulation results are shown in Figure 4. The resource utilization to implement the Walsh codes are tabulated in Table 2.

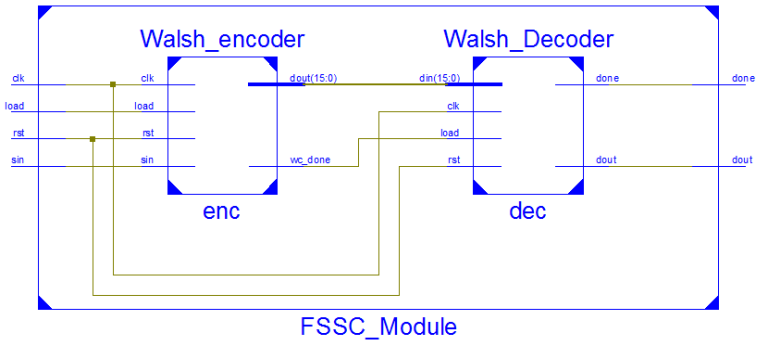

Figure.3: Internal Architecture of Walsh encoder and decoder unit

Figure 4 shows the simulation results for the WC Module employing encoder and decoder units. A lower reset (rst) and a high load signal activate the global clock (clk). Based on WM module operation, the 1-bit Data input (sin) is fed in a sequence, and the data output (dout) is obtained after 10.5 clock cycles.

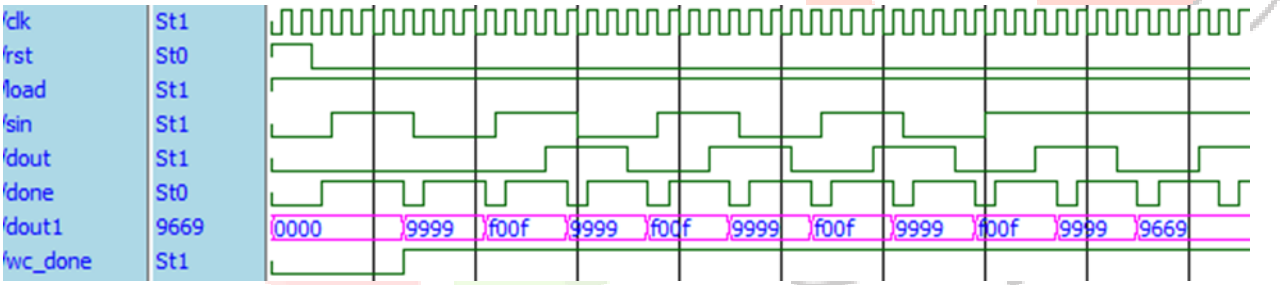

Figure. 4: Simulation results of Walsh encoder and decoder

Table 2: Resource utilization of WC module on Artix-7 FPGA

Constraint	Resources	Walsh Code module
Chip Area	Slices	37
	LUTs	78
	FF pairs	27
Time	Minimum Period (ns)	3.472
	Max. Frequency (MHz)	288.035
Power	Static Power (mW)	82
	Dynamic Power (mW)	5
	Total Power (mW)	87

The implemented Walsh code scheme is compared with the other existing Schemes. This scheme utilizes 37 slices, 78 LUTs and the total power consumed is 87mW with a maximum frequency of 288.035MHz. The comparative analysis of Walsh codes with other techniques from literature is tabulated in Table 4.

Table 3: Comparison of Different Coding techniques on Different FPGA's

Coding Techniques	FPGA Devices	Slices	LUTs	Max. Frequency (MHz)
RS Codec [11]	Virtex-4	2014	3652	152.592
LDPC Codec [12]	Virtex-5	720	913	319
Viterbi Codec [13]	Virtex-7	198	390	393.5
BCH Codec [14]	Virtex-5	144	220	268.962
Golay Codes [15]	Virtex-4	230	785	195.082
Turbo Codes [16]	Virtex-5	113	206	NA
Walsh Codes [Present Work]	Artix-7	37	78	288.035

The proposed Walsh codes are implemented on Artix-7 FPGA device, which utilizes 78 look-up tables ,37 slices and has a frequency of 288.03 MHz.The suggested Walsh codes outperform existing Coding techniques in terms of Chip area (Slices, LUTs) and Operating Frequency [11-16]. The coding techniques discussed above are appropriate for use in sophisticated, long-distance, high-data-rate communication systems. Walsh Coding techniques are more suited to low-bandwidth, short-range wireless communication and HBC systems.

VI. Conclusion

The Walsh codes is designed and implemented on Artix-7 FPGA for HBC communication system. The advantages and limitations are FEC coding techniques were summarized. The designed Walsh code module showed a power consumption of 87mW which is an improvisation as compared to the other reported techniques. The resource utilization is also less in comparison to the other convolution codes and block codes. The Walsh codes are used in IEEE802.15.6 based transceivers which achieve better data rates with reduced complexity.

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