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ORIGINAL ARTICLE

A New Five-Level Diode Clamp Multilevel Inverter Topology

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ABSTRACT

This paper presents a new five level diode clamped multilevel inverter topology which can be used for low-medium power industrial applications. In this work proposes single phase five level Diode Clamped Multilevel Inverter (DCMLI) topology using an auxiliary switch is presented, the number of power devices required to implement a five-level output. The topology is tested in the design of a 5 levels diode clamp multilevel inverter simplified; circuit operation is presented, simulated and validated with experimental tests performed on a laboratory prototype. In this paper, the concept of a 5-level diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible. The simulation result, the output voltage waveform presents better harmonics profile.

Keywords—*Diode clamp multilevel inverter, Total harmonic distortion, Single-phase induction motor control.*

1. INTRODUCTION

Recently, single-phase induction motor is widely used in buildings and industries because of its compact size, endurance and cheap price. However, industrial sector requires improving its efficiency by employing various controls to improve the efficiency and to save energy. In this paper, the concept of a 5-level diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible. Therefore, controlling approach of voltage and frequency supplied to stator coil in order to control the motor speed efficiently according to actual operations which was developed by [1-2] is employed. In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. The inverters with voltage level 3 or more are referred as multi level inverters. Multilevel inverters have become attractive recently particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage. New diode clamping multilevel inverter. Developed DC link capacitor voltage balancing in a three phase diode clamped inverter controlled by a direct space vector of line to line voltages. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

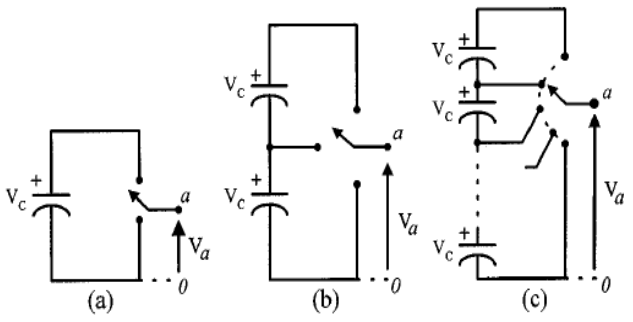

Figure.1: One Phase Leg Of An Inverter With (A) Two Levels, (B) Three Levels, And (C) N Levels.

2. MULTILEVEL INVERTER TOPOLOGY

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.

The main multilevel topologies are classified into three categories:

- diode clamped inverters
- flying capacitor inverters
- cascaded inverters

In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure.

The diode-clamp inverter type is used for experimentations in this article. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading. The diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible.

2.1 DIODE-CLAMP MULTILEVEL INVERTER

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is *Vdc*. An *n* level inverter needs (*n*-1) voltage sources, 2(*n*-1) switching devices and (*n*-1) (*n*-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform.

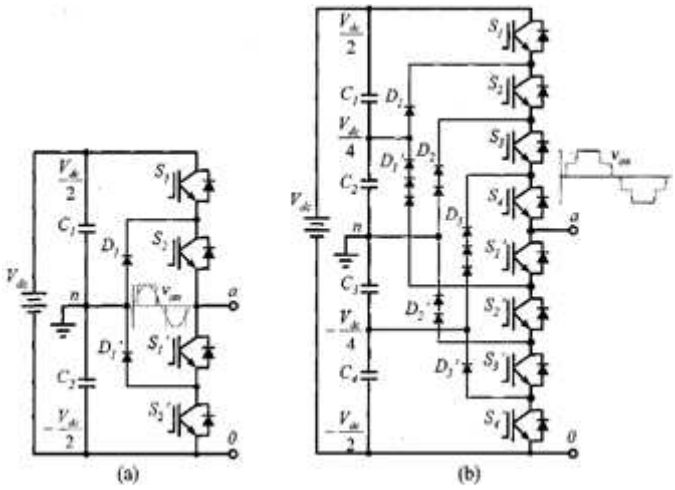

Figure.2: Diode-Clamped Multilevel Inverter Circuit Topologies. (A) Three-Level. (B) Five-level

Figure.2(a) shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/2$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/2$ through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

1. Voltage level $V_{an}= V_{dc}/2$, turn on the switches S1andS2.
2. Voltage level $V_{an}= 0$, turn on the switches S2 and S1′.
3. Voltage level $V_{an}= - V_{dc}/2$ turn on the switches S1′,S2′.

Figure.2 (b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes. The order of numbering of the switches for phase a is S1, S2, S3, S_4, S_1', S_2', S_3' and S_4'.

For example to have $V_{dc}/2$ in the output, switches S1 to S4 should conduct at the same time. For each voltage level four switches should conduct. As it can be seen in Table.1 the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped

multilevel inverter. This problem can be solved by using a two times voltage source or cascading two diode clamped multilevel inverters. The output voltage of a 5-level diode clamped multilevel inverter all of the voltage level should have the same voltage value.

The switching angles should be calculated in such a way that the THD of the output voltage becomes as low as possible. The switching angle calculation method that is used in this thesis is the harmonic elimination method. In this method the lower dominant harmonics can be eliminated by choosing calculated switching angles. Table-1 shows the output voltage levels and the corresponding switch states for one phase of the chosen five level DCMLI. The switches are arranged into 4 pairs (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), (S_4, S_4'). If switching sequence as

given in table 1. State condition 1 means switch ON and 0 means switch OFF.

V_0	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table1: The switching state of diode clamp multilevel inverter.

The steps to synthesis the five level phase a output voltage in this work are as follows:

1. For phase a output voltage of $V_{an}=0$, two upper switches S_3, S_4 and two lower switches S_1' and S_2' are turned on.

2. For an output voltage of $V_{an}=V_{dc}/4$, three upper switches S_2, S_3, S_4 and one lower switch S_1' are turned on.

3. For an output voltage of $V_{an}=V_{dc}/2$, all upper switches S_1 through S_4 are turned on.

4. To obtain the output voltage of $V_{an}= -V_{dc}/4$, upper switch S_4 and three lower switches S_1', S_2' and S_3' are turned on.

5. For an output voltage of $V_{an} = -V_{dc}/2$, all lower switches S_1' through S_4' are turned on.

The phase a output voltage Van has five states: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$. The gate signals for the chosen five level DCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices.

3. REDUCED SWITCHING TOPOLOGY

For practical implementation, the switching state needs to be converted into transistor signals. Once the transistor signals are established, general expressions for the a-phase line to ground voltage & the a-phase component of the DC currents can be written as

$$V_{ao}= H_{an}V_{n0}+ H_{an-1}V_{n-10}+\ldots..+H_{a1}V_{10} \quad (1)$$

$$V_{bo}= H_{bn}V_{n0}+ H_{bn-1}V_{n-10}+\ldots..+H_{b1V10} \quad (2)$$

$$V_{co}= H_{cn}V_{n0}+ H_{cn}\text{-}1V_{n-10}+\ldots..+H_{c1V10} \quad (3)$$

The Node Currents for the "n" level inverter are given by

$$I_n = H_{an}I_a+H_{bn}I_b+H_{cn}I_c$$

$$I_{n-1} = (H_{an-1})I_a+(H_{bn-1})I_b+(H_{cn-1})I_c$$

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$$I_1 = H_{a1}I_a+H_{b1}I_b+H_{c1}I_c \quad (4)$$

The above relationships may be programmed into simulation software that simulates one phase of a diode clamped inverter. A number of blocks can be connected together for a multiphase system. For more simulation details, the transistor & diode KCL & KVL equations may be implemented. This allows inclusion of the device voltage drops & also the individual device voltages & currents.

To express this relationship, consider the general N level diode clamped structure. Through the clamping action of diodes, the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank. Finally the capacitor junction currents may be expressed as the difference of two clamping diode currents. In case of a five level inverter, the expression reduces to

$$C1pVc1 = -Idc+Ha3Ia+Hb3Ib+Hc3Ic \quad (5)$$

$$C1pVc2 = -(Idc+Ha1Ia+Hb1Ib+Hc1Ic) \quad (6)$$

4. SIMULATION RESULTS

The simulation results obtained for a five level multilevel inverter as given below:-

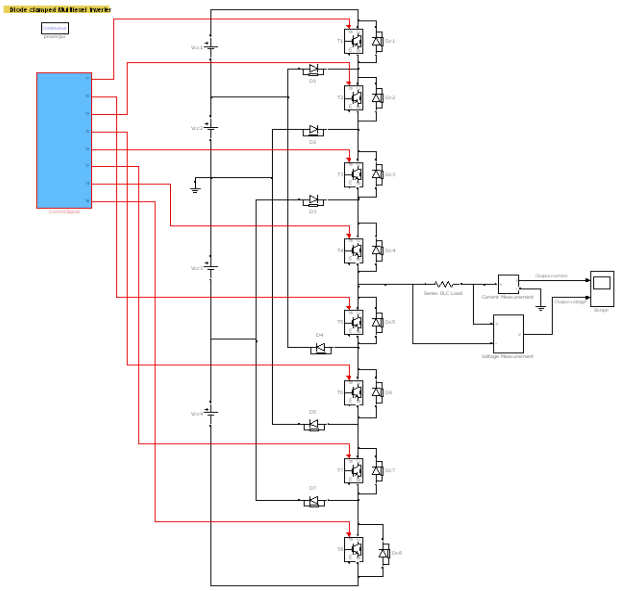
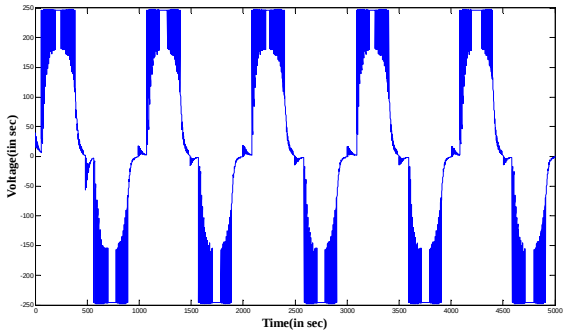
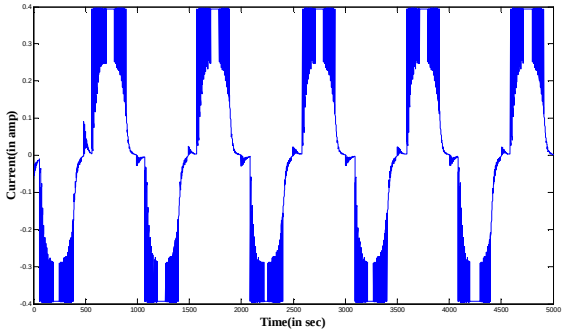


Figure3: Simulink Model of a Five Level DCMI.

RESULTS:



(A) OUTPUT VOLTAGE



(B) OUTPUT CURRENT

Figure 4: Output Voltage & Current of a Five Level DCMI.

5. CONCLUSION

This paper has presented a new topology for the diode clamped multilevel inverter. This multilevel topology has been presented for industrial application. The working of the inverter is explained in detail. The main concept of this inverter is to use diodes to limit the power devices voltage stress. The diode clamp multilevel inverters have become an effective and practical solution for largest output levels and the smallest Total Harmonics Distortion percentage. The simulation result, the output voltage waveform presents better harmonics profile.

NOMENCLATURE

In Above Simulation Results:
Figure 1&2 represents the variations in output voltage of a 3level multilevel inverter where
X axis-.Time in sec.
Y axis- Phase Voltage & Current.
Vdc- DC bus voltage.(between capacitor & switch)
DCMLI- Diode clamp multilevel inverter.
THD- Total Harmonic Distortion.

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