SINGLE SWITCHED HIGH GAIN QUADRATIC BOOST CONVERTER WITH REDUCED VOLTAGE STRESS

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***Abstract*—A High Gain Single Switched Quadratic Boost converter architecture is presented for low-voltage renewable and portable energy systems requiring efficient voltage amplification, reduced semiconductor stress, and compact passive components. The proposed topology combines an active switched-inductor network with a multi-stage charge-pump mechanism to achieve substantial voltage boosting without the need for extreme duty ratios. The coordinated energy transfer between inductors and capacitors enables improved conversion efficiency, reduced conduction losses, and enhanced voltage gain. Volt–second balance formulation and capacitor charge analysis provide closed-form expressions for voltage gain, device stresses, and component sizing. The performance of the converter is validated through MATLAB/Simulink simulations, confirming the analytical predictions. Owing to its high step-up capability and improved efficiency, the proposed design is well-suited for renewable interfaces, electric mobility subsystems, and distributed DC microgrid applications. Results are obtained by simulating the converter in MATLAB/Simulink R2024a. The simulation results show that the proposed high-gain converter delivers high voltage gain with reduced voltage stress across the switching devices and achieves a maximum operating efficiency of 76%. A hardware with an input voltage of 5V is implemented using the TMS320F28335 microcontroller where output voltage of 22.8V is achieved, corresponding to a voltage gain of 4.54. Additionally, a secondary output voltage of 15.8V is obtained under the same input conditions, corresponding to a voltage gain of 3.17, thereby experimentally validating the multi-output capability of the proposed converter.**

***Index Terms*—Boost Converter, Gain, Efficiency.**

I. INTRODUCTION

The rapid advancement of modern electrical and electronic systems has significantly increased the demand for efficient and high-gain DC–DC power conversion. Applications such as electric vehicles, renewable energy systems, portable electronics, LED drivers, and distributed DC microgrids require compact, reliable, and high step-up converters capable of delivering stable output voltages from low-voltage sources. In particular, low-power applications in the range of 10 W demand simple, cost-effective, and efficient converter topologies with reduced component count and minimal control complexity.

Conventional boost converters are widely adopted due to their simple structure and ease of control. However, they exhibit inherent limitations under high voltage gain requirements. Achieving large step-up ratios necessitates operation at extreme duty cycles, which leads to increased conduction losses, elevated switching stress, severe diode reverse-recovery problems, and significant output voltage ripple. These issues degrade efficiency and reliability, making conventional boost converters less suitable for high-gain applications.

To address these limitations, various high-gain converter topologies have been proposed in the literature. In [1], an improved voltage-mode controlled quadratic converter enhances stability, although control complexity persists. In [2], a switched-capacitor-assisted quadratic converter achieves high gain with reduced ripple at the cost of increased components. Enhanced gain buck–boost converters in [3], [4] provide quadratic gain with continuous current characteristics but require multiple switches. Soft-switching approaches in [5], [6] reduce switching losses while introducing auxiliary or resonant elements. Capacitor-clamped structures in [7] lower voltage stress but increase circuit complexity, whereas Z-network, dual-switch, and hybrid energy pumping converters in [8] improve voltage gain with added implementation challenges. Modified and quasi-Z-source converters in [9], [10], [11] achieve higher gain with reduced components, though their control design remains complex. Quadratic and switching-capacitor-based converters in [12], [13] provide common-ground operation and reduced ripple but involve higher-order dynamics. Dual-output converters in [14], [15], [16] enhance flexibility and gain, albeit with increased design complex-

ity. Furthermore, high-gain converters with soft-switching in [17], [18] and bidirectional switched-inductor converters in [19] offer improved efficiency and operational versatility, but require additional passive elements and complex configurations, while [20] presents a dual-output quadratic boost converter with high gain, reduced stress, and continuous input current validated through simulation and hardware.

Despite these advancements, most existing converters suffer from high component count, complex control strategies, increased voltage stress, or limited efficiency, particularly in low-power applications.

In recent years, non-isolated high-gain converter topologies with single-switch configurations have attracted considerable attention due to their ability to achieve high voltage conversion ratios with reduced control complexity. By integrating switched-inductor structures with quadratic boosting techniques, such converters can deliver high voltage gain at moderate duty cycles while maintaining continuous input current characteristics. These features make them highly suitable for photovoltaic systems, fuel cells, battery-powered applications, and other low-voltage renewable energy sources.

This work presents the design and analysis of a single-switch high-gain quadratic boost converter tailored for low-power applications. The proposed topology aims to achieve high voltage gain, reduced output voltage ripple, minimized switching stress, and efficient utilization of passive components. Additionally, the converter is capable of supporting multiple output terminals, enabling the generation of different voltage levels from a single input source.

Furthermore, the converter operates effectively in continuous conduction mode (CCM), ensuring reduced input current ripple and improved compatibility with source characteristics. By optimizing the energy transfer mechanism through proper coordination of inductors and capacitors, the proposed design enhances voltage boosting capability without requiring extreme duty cycles. This results in improved efficiency, reduced thermal stress, and enhanced system reliability.

The performance of the proposed converter is validated through detailed simulation and experimental investigation under low-power operating conditions. Both steady-state and dynamic characteristics, including voltage gain, efficiency, ripple content, and switching stress, are analyzed to verify the effectiveness of the design. The results demonstrate that the proposed single-switch high-gain quadratic boost converter provides a practical and efficient solution for modern low-power, high-gain DC–DC conversion applications.

Moreover, the use of a single active switch simplifies the gate driving circuit and reduces control complexity, making the topology particularly advantageous for low-power systems. The ability to generate multiple output voltage levels from a single input source further eliminates the need for additional conversion stages. Reduced output voltage ripple and lower semiconductor stress enable the use of cost-effective components while improving overall reliability.

Therefore, the proposed converter offers a cost-effective, efficient, and scalable solution for high-gain DC–DC conversion, making it suitable for photovoltaic systems, battery-powered applications, and other emerging low-voltage energy systems.

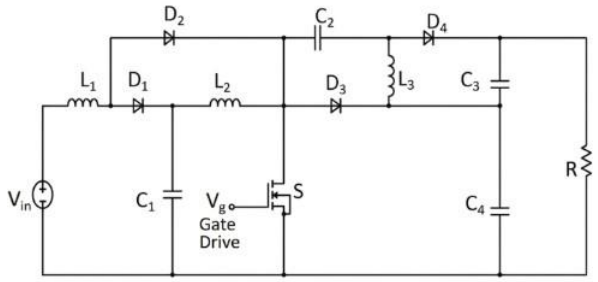

Fig. 1. High Gain switched LC Converter

A. Modes of Operation

The High Gain LC converter operates primarily in two modes.

1) Mode 1: In Mode 1, the switch S is turned ON, causing diode D_2 to conduct while diodes D_1, D_3 and D_4 remain reverse-biased. During this interval, inductor L_1 draws energy directly from the input source V_{in} and begins charging. Capacitor C_1 transfers its energy to inductor L_2, allowing L_2 to charge simultaneously. In the active switched-inductor branch, inductor L_3 charges using the energy supplied from capacitor C_4 through diode D_2. Throughout this period, capacitors C_3 and C_4 continue to support the load, ensuring continuous output current. Thus, Mode-I serves as the main energy accumulation phase, where all inductors store energy while the output is maintained by the capacitor network. Figure 2 shows the operating circuit of mode 1.

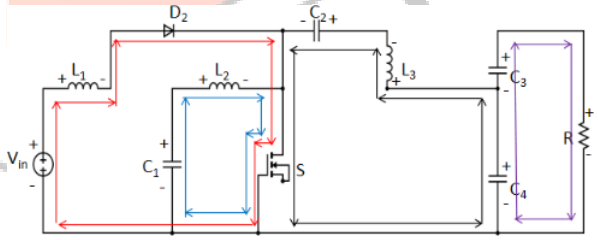

Fig. 2. Operating circuit of of Mode 1

By applying KVL,

$$V_{L2} = V_{C1} \quad (1)$$

$$V_{L3} = V_{C4} - V_2 \quad (2)$$

$$V_0 = V_{C3} + V_{C4} \quad (3)$$

By applying KCL,

$$i_{in} = i_{L1} \quad (4)$$

$$i_{C1} = i_{L2} \quad (5)$$

$$i_{L1} + i_{C2} - i_{L2} = i_S \quad (6)$$

$$i_{C4} - i_{L3} = i_0 \quad (7)$$

$$i_{C3} = i_0 \quad (8)$$

2) Mode 2: During Mode 2 operation, the switch S is turned OFF. As a result, diodes D_1, D_3, and D_4 become forward biased, while diode D_2 remains reverse biased due to the polarity reversal across it. In this interval, all inductors release their stored energy. Inductor L_1 discharges through diode D_1 and transfers its to charge capacitor C_1. Simultaneously, inductor L_2 discharges through diode D_3, contributing to the energy transfer towards the output side and charging capacitor C_4. At the same time, inductor L_3, which was previously energized during the ON state, discharges through diode D_4 and charges capacitor C_3. The capacitors C_2 and C_3 together help in boosting the output voltage by forming a stacked voltage configuration. The load is supplied by the combined energy of capacitors C_3 and C_4 along with the discharging inductors. This mode is responsible for achieving high voltage gain, as multiple energy storage elements simultaneously transfer energy to the output. Thus, Mode 2 represents the energy delivery phase of the converter, where inductors release stored energy and capacitors support the boosted output voltage. Figure 3 shows the operating circuit of mode 2.

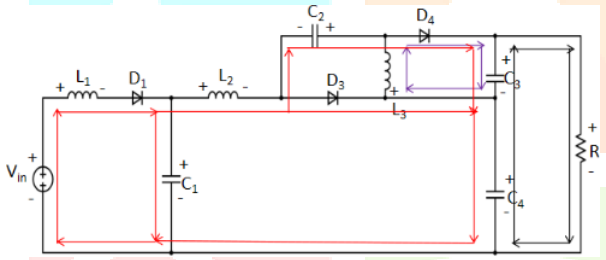

Fig. 3. Operating circuit of of Mode 2

By applying KVL,

$$V_{in} - V_{L1} - V_{C1} = 0 \quad (9)$$

$$V_{in} - V_{L1} - V_{L2} - V_{C4} = 0 \quad (10)$$

$$V_{in} - V_{L1} - V_{L2} + V_{C2} - V_{C3} - V_{C4} = 0 \quad (11)$$

$$-V_{L3} - V_{C3} = 0 \quad (12)$$

$$V_{C3} + V_{C4} = V_0 \quad (13)$$

By applying KCL,

$$i_{in} = i_{L1} \quad (14)$$

$$i_{L1} - i_{C1} - i_{L2} = 0 \quad (15)$$

$$i_{C4} + i_{L3} - i_{C3} = 0 \quad (16)$$

$$i_{C3} = i_0 \quad (17)$$

Figure 4 illustrates the theoretical waveforms corresponding to Mode 1 and Mode 2.

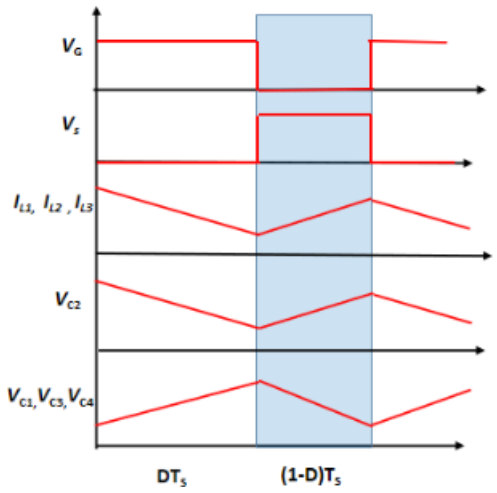

Fig. 4. Theoretical waveform

B. Design of Components

The input voltage is taken as $V_{in} = 15$ V, and the converter is designed to produce an output voltage of $V_o = 100$ V with an output power of $P_o = 10$ W. The switching frequency is selected as $f_s = 30$ kHz considering a trade-off between switching losses and passive component size.

The load resistance is calculated as:

$$R_o = \frac{V_o^2}{P_o} = \frac{100^2}{10} = 1000\,\Omega \quad (18)$$

Using the voltage gain relation,

$$\frac{V_o}{V_{in}} = \frac{1+D}{(1-D)^2} \quad (19)$$

$$D = 0.52 \quad (20)$$

The output current is:

$$I_o = \frac{V_o}{R_o} = \frac{100}{1000} = 0.1\,\text{A} \quad (21)$$

The inductors are designed assuming 25% current ripple to ensure continuous conduction mode (CCM), reduced current stress, and improved efficiency.

$$I_{L1} = I_{in} = \frac{V_o I_o}{V_{in}} = \frac{100 \times 0.1}{15} = 0.66\,\text{A} \quad (22)$$

$$L_1 \geq \frac{DV_{in}}{\Delta i_{L1} f_s} = \frac{0.52 \times 15}{0.16 \times 30000} \approx 1.8\,\text{mH} \quad (23)$$

$$I_{L2} = \frac{(1+D)I_o}{1-D} = \frac{1.52 \times 0.1}{0.48} = 0.31\,\text{A} \quad (24)$$

$$L_2 \geq \frac{DV_{in}}{\Delta i_{L2}(1-D) f_s} = \frac{0.52 \times 15}{0.079 \times 0.48 \times 30000} \approx 8\,\text{mH} \quad (25)$$

$$I_{L3} = I_o = 0.1\,\text{A} \quad (26)$$

$$L_3 \geq \frac{DV_{in}}{\Delta i_{L3}(1-D)f_s} = \frac{0.52 \times 15}{0.025 \times 0.48 \times 30000} \approx 22\,\text{mH} \quad (27)$$

The capacitors are designed based on 1% voltage ripple criterion to ensure low output voltage ripple and improved voltage regulation.

$$V_{C1} = \frac{V_{in}}{1-D} = \frac{15}{0.48} = 31.25\,\text{V} \quad (28)$$

$$C_1 \geq \frac{D(1+D)V_o}{\Delta V_{C1}(1-D)R_o f_s} \approx 17.7\,\mu\text{F} \quad (29)$$

$$V_{C2} = V_{C3} = \frac{DV_{in}}{(1-D)^2} = 33.85\,\text{V} \quad (30)$$

$$C_2, C_3 \geq \frac{DV_o}{\Delta V_{C2}R_o f_s} \approx 5.1\,\mu\text{F} \quad (31)$$

$$V_{C4} = \frac{V_{in}}{(1-D)^2} = 65.10\,\text{V} \quad (32)$$

$$C_4 \geq \frac{(2+D)V_o}{\Delta V_{C4}R_o f_s} \approx 5.33\,\mu\text{F} \quad (33)$$

Thus, the selected values are:

$L_1 = 1.8\,\text{mH}, 1\,\text{A}$ $L_2 = 8\,\text{mH}, 1\,\text{A}$ $L_3 = 22\,\text{mH}, 1\,\text{A}$

$C_1 = 22\,\mu\text{F}, 100\,\text{V}$ $C_2 = C_3 = 22\,\mu\text{F}, 100\,\text{V}$

$C_4 = 22\,\mu\text{F}, 100\,\text{V}$

All components are chosen to maintain continuous conduction mode (CCM), minimize current and voltage ripple, lower switching and conduction losses, and ensure stable operation under steady-state conditions with acceptable voltage stress on semiconductor devices. Furthermore, passive elements such as inductors and capacitors are properly designed to sustain energy transfer balance and reduce transient variations during switching transitions.

II. Simulations and Results

TABLE I
Simulation Parameters of Modified Boost Converter

Parameters	Value
Input voltage, V_{in}	15 V
Output voltage, V_O	100 V
Output load, R	1000 Ω
Switching frequency, f_s	30 kHz
Inductance, L_1	1.8mH, 1A
Inductance,L_2	8mH,1A
Inductance, L_3	22mH,1A
Capacitance C_1,C_2,C_3	22μF, 60V
Capacitance C_4	22μF, 100V
Duty Cycle	52%

Figure 5 shows the input voltage and input current.

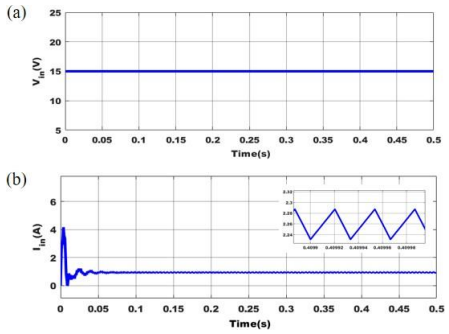

Fig. 5. (a) Input Voltage (V_{in}) and (b) Input Current (I_{in})

It is observed that the input voltage V_{in} is 15V and the input current I_{in} is 0.9A, while the switching frequency is set at 30kHz. The output voltage and current waveforms corresponding to the two output terminals are illustrated in the subsequent figures. Figure 6 presents the output voltage and output current across the first terminal.

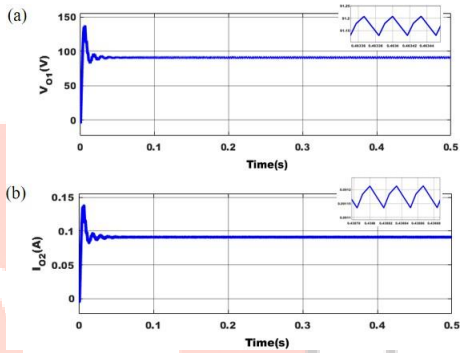

Fig. 6. (a) Output Voltage (V_{01}) and (b) Output Current (I_{01})

The output voltage V_{01} is 91.34V with ΔV_{01} = 0.08V and the output current I_{01} is 0.091A with ΔI_{01} = 0.00008A

Figure 7 shows the output voltage and output current across the second terminal.

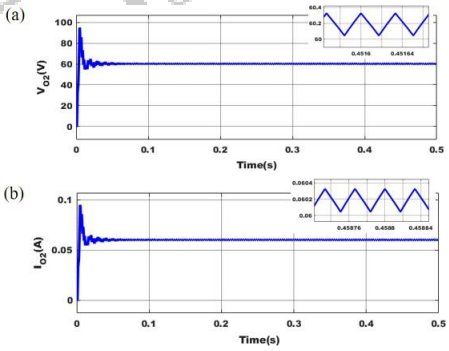

Fig. 7. (a) Output Voltage (V_{02}) and (b) Output Current (I_{02})

It can be seen that the output voltage V_{02} is 60.45V with ΔV_{02} = 0.28V, and the output current I_{02} is 0.06A with ΔI_{02} = 0.0004A.

Figures 8 illustrates the gate drive signals and the voltage stresses experienced by the switch in the converter circuit.

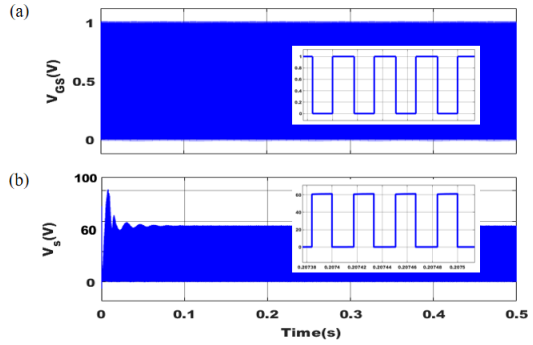

Fig. 8. Gate Pulse (V_{GS}) and Voltage Stress (V_S) of switch S

The measured voltage stress across switch S is 61.16V. Figure 5.9 shows the currents through inductor L_1,L_2 and L_3.

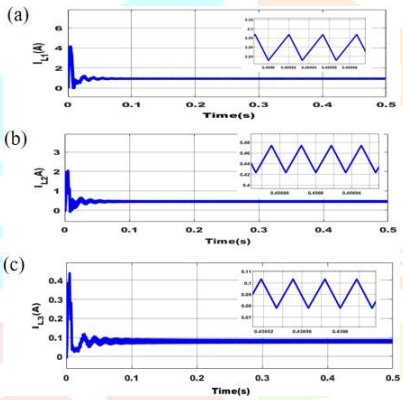

Fig. 9. Current across Inductance (a)i_{L1} (b)i_{L2} (c)i_{L3}

It can be seen that the current through inductor L_1 is 1.959A, L_2 is 0.78A and through L_3 is 0.14A. Figure 10 shows the voltage across three capacitors, V_{C1}, V_{C2}, V_{C3} and V_{C4}

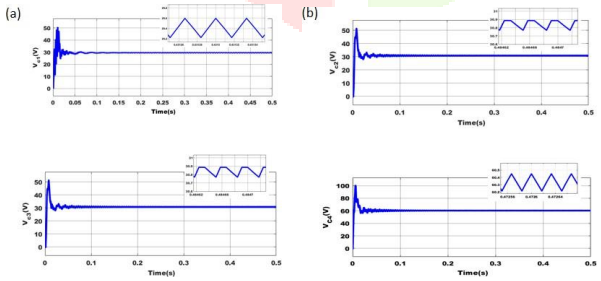

Fig. 10. Voltage across Capacitors (a) V_{C1} and V_{C3}, (b) V_{C2} and V_{C4}

It can be seen that Voltage across capacitor C_1 is 29.59V. Voltage across capacitor C_2 is 30.88V and voltage across capacitor C_3 is 30.88V and C_4 is 60.45V.

III. Performance Analysis

Efficiency of a power equipment is defined at any load as the ratio of the power output to the power input. The efficiency tells us the fraction of the input power delivered to the load. Here the efficiency vs output power with R load and RL load done for quadratic boost converter (for R = 1000Ω) and high gain modified quadratic boost converter (for R = 1000Ω) and graphs are shown in Figure 5.13. The maximum efficiency of high gain boost converter is around 78% for an output power of 10W for R load and 76% for RL load for an output power of 200W.

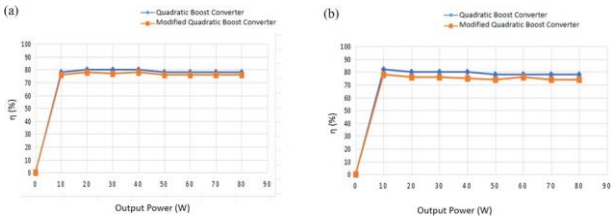

Fig. 11. Efficiency Vs Output Power for (a) R load (b) RL load

The plot of gain of the converter as a function of duty ratio is shown in Figure 12. By analyzing the graph, it is clear that the voltage gain increases with duty ratio. It is observed that the voltage gain of the single switched high gain quadratic boost converter increases at a higher rate than the single switched quadratic boost converter for the same duty ratio. This is due to the additional energy transfer paths and enhanced voltage boosting mechanism present in the modified topology. Hence, the proposed converter is more suitable for applications requiring high step-up voltage gain at lower duty ratios.

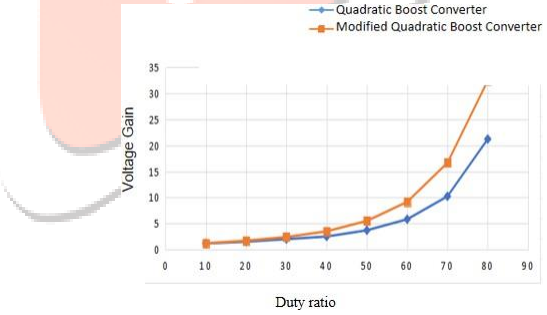

Fig. 12. Voltage gain Vs Duty ratio

The plot in Fig. 5.16 shows that output voltage ripple increases with duty ratio. The modified high-gain quadratic boost converter exhibits a slightly higher rate of increase compared to the conventional converter due to higher energy transfer and voltage levels. However, the ripple remains within acceptable limits and can be reduced further with proper output filter design. Additionally, the increase in ripple at higher duty ratios highlights the importance of optimized component selection for maintaining stable converter performance.

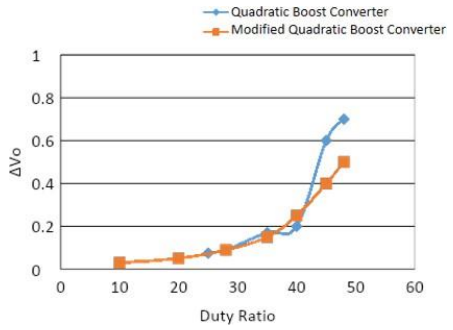

Fig. 13. Output Voltage Ripple VS Duty Ratio

Figure 14 depicts the redesigned high gain converter's output voltage ripple behavior in response to varied switching frequency. The output voltage ripple decreases as the switching frequency increases. This is because higher switching frequency reduces the energy storage interval in passive components, resulting in smoother output voltage. Hence, operating at higher switching frequencies improves output voltage quality, although it may lead to increased switching losses. Therefore, an optimal switching frequency must be selected to achieve a balance between reduced ripple and overall converter efficiency.

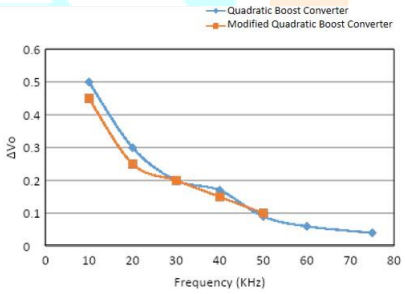

Fig. 14. Output voltage ripple VS frequency

IV. Comparitive Study

Table 2 presents a comparison between the conventional Quadratic Boost converter and the proposed topology under identical operating conditions of 15 V input voltage and 30 kHz switching frequency. The results indicate that, for the same duty ratio, the proposed converter achieves a substantial increase in voltage gain from 4.3 to 6.85. This improvement is primarily attributed to the enhanced energy transfer process and the inclusion of additional boosting stages in the modified design. Furthermore, the higher gain is achieved without operating at extreme duty ratios, which contributes to improved efficiency and reduced stress on the switching components. Consequently, the proposed converter exhibits improved suitability for high step-up conversion applications. In addition, the enhanced topology ensures superior voltage regulation and maintains stable operation under varying load conditions. It also leads to lower current ripple and improved overall output power quality.

TABLE II
Comparison between quadratic Based Boost Converter& High Gain Quadratic Boost Converter

Parameters	Conventional boost converter	Quadratic Boost Converter	Modified Quadratic Boost Converter
No. of Switches	1	1	1
No. of Inductors	1	2	3
No. of Capacitors	1	2	4
Voltage Gain	1.375	4.3	6.597
Voltage stress across switch	66.56V	92.58V	61.16.V
Input Current ripple	0.2A	0.05A	0.05 A
Output Voltage ripple	0.1V	0.15V	0.08V
Output Current ripple	0.0025A	0.00015A	0.00008A

Table 3 provides a detailed comparison of the components used in the proposed High gain single switched quadratic boost converter against those in other converter designs.

TABLE III
Comparison between High Gain quadratic boost Converter & Other converters

Converter	Boost converter in [2]	Boost converter in [3]	Boost converter in [4]	High Gain Quadratic Boost converter
No. of Switches	3	2	2	1
No. of Diodes	1	2	5	4
No. of Inductors	3	3	2	3
No. of Capacitors	2	3	5	4
Power	150 W	40 W	150 W	10W
Voltage Gain	$\frac{1}{(1-D)^2}$	$\frac{D^2}{(1-D)^2}$	$\frac{3+D}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}$

V. Experimental Setup with Result

A. Hardware Implementation

For hardware implementation, the input voltage is set to $V_{in} = 5$ V. The switching pulses are generated using the TMS320F28335 microcontroller, which provides precise control of the duty ratio and switching frequency. The converter is operated at a switching frequency of $f_s = 30$ kHz with a duty ratio of $D = 0.52$. The power switch used is the IRFB4110 MOSFET, selected due to its low on-state resistance and suitability for high-frequency operation with relatively low voltage rating. The gate driver circuit is implemented using the TLP250H optocoupler, which provides electrical isolation between the control and power circuits, and ensures proper gate driving capability for reliable switching. The experimental setup of the single-switched high gain quadratic boost converter with multiple output configuration consists of a DC input source, control unit, driver circuit, and power stage. The microcontroller generates PWM pulses which are fed to the TLP250H driver to control the MOSFET switching. In this configuration, the converter produces two output voltages from

a single input source. For an input of 5 V, the obtained output voltages are:

$$V_{o1} = 22.8\,\text{V}, \quad V_{o2} = 15.7\,\text{V}$$

The output voltages are measured using a digital storage oscilloscope (DSO). The overall efficiency of the converter is found to be approximately 78%, considering conduction and switching losses. The use of a low-rated switch operating at high frequency reduces the size of passive components while maintaining high voltage gain. The results validate the performance of the proposed converter in achieving multiple boosted outputs with stable operation and acceptable efficiency. The experimental configuration of single switched high gain modified quadratic boost converter and output voltage waveforms are shown below. For a 5V input voltage, 22.8V output voltage is produced.

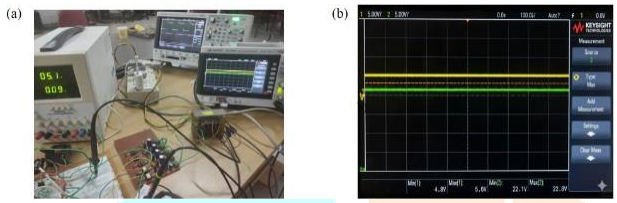

Fig. 15. (a) Experimental Setup 1 (b) Output Voltage(V_{O1}) of Converter

The experimental configuration and output voltage waveforms with the same input voltage are shown below, where 15.8V output voltage is obtained.

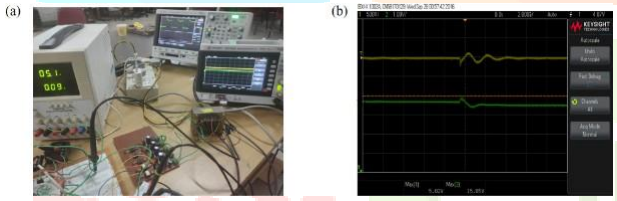

Fig. 16. (a) Experimental Setup 2 (b) Output Voltage(V_{O2}) of Converter

VI. Conclusion

This research demonstrates a high-gain quadratic boost converter architecture that effectively mitigates switch voltage stress through the integration of switched-inductor and voltage-multiplier techniques. The proposed topology achieves high voltage gain at moderate duty cycles, thereby reducing stress on switching devices while maintaining a stable output with low ripple. Compared to conventional DC–DC boost converters, the proposed design offers improved voltage gain, enhanced reliability, and better overall efficiency. Simulation results validate the performance, showing an efficiency of 80% for the primary converter at 10 W output, while the modified configuration achieves a peak efficiency of 78% under identical conditions. Furthermore, the converter exhibits reduced input current ripple and lower conduction losses, enabling the use of low-rated and cost-effective passive components in a compact design. The multi-output capability allows simultaneous generation of multiple voltage levels from a single input source, providing flexibility for diverse load requirements. With fast transient response and stable operation without extreme duty cycles, the proposed converter serves as an efficient and practical solution for fuel cells and low-voltage renewable energy applications.

References

[1] C.-Y. Chan, "An improved voltage-mode controller for the quadratic boost converter," ***IEEE Transactions on Circuits and Systems***,Express Briefs,Vol. 69, no. 2, February 2022.

[2] N. Korada, "Novel quadratic high gain boost converter with adaptive soft-switching scheme and reduced conduction loss," ***IEEE Transactions on Industrial Electronics***, Vol. 58, no. 6, November/December 2022.

[3] M. Veerachary, "Design and analysis of two-switch-based enhanced gain buck–boost converters," ***IEEE Transactions on Industrial Electronics***, Vol. 69, No. 4, April 2022.

[4] Naresh K, "A novel high quadratic gain boost converter for fuel cell electric vehicle applications," ***IEEE Journal of Emerging and Selected Topics in Industrial Electronics***, Vol. 4, no. 2, April 2023.

[5] H. Bi, P. Wang, and Y. Che, "A capacitor clamped H-type boost DC–DC converter with wide voltage-gain range for fuel cell vehicles," ***IEEE Transactions on Vehicular Technology***, vol. 68, no. 1, pp. 276–290, Jan. 2019.

[6] P. Kumar and M. Veerachary, "Z-network plus switched capacitor boost DC-DC converter," ***IEEE Journal of Emerging and Selected Topics in Power Electronics***, vol. 9, no. 1, pp. 791–803, Feb. 2021.

[7] M. Veerachary and P. Sen, "Design and analysis of dual-switch enhanced gain boost converter," in ***IEEE International Conference on Computing, Power and Communication Technologies***, 2020, pp. 83–89.

[8] K. I. Hwu and W. C. Tu, "Voltage-boosting converters with hybrid energy pumping," ***IET Power Electronics***, vol. 5, no. 2, pp. 185–195, 2020.

[9] J. Liu, J. Wu, J. Qiu, and J. Zeng, "Switched Z-source/quasi-Z-source DC–DC converters with reduced passive components for photovoltaic systems," ***IEEE Access***, vol. 7, pp. 40893–40903, 2019.

[10] L. Yang, D. Qiu, B. Zhang, G. Zhang, and W. Xiao, "A modified Z-source DC–DC converter," in ***Proceedings of the 16th European Conference on Power Electronics and Applications***, 2018, pp. 1–9.

[11] M. Veerachary and P. Kumar, "Analysis and design of fourth-order quasi-Z-source equivalent DC–DC boost converter," in ***IEEE Transportation Electrification Conference and Expo***, 2019, pp. 1–6.

[12] S. A. Gorji, A. Mostaan, H. T. My, and M. Ektesabi, "Non-isolated buck-boost DC–DC converter with quadratic voltage gain ratio," ***IET Power Electronics***, vol. 12, no. 6, pp. 1425–1433, Feb. 2019.

[13] S. A. Gorji, A. Mostaan, H. T. My, and M. Ektesabi, "Non-isolated buck-boost dc-dc converter with quadratic voltage gain ratio," ***IET Power Electronics***, vol. 12, no. 6, pp. 1425–1433, Feb. 2019.

[14] M. Veerachary and V. Khubchandani, "Analysis, design and control of switching capacitor based buck-boost converter," ***IEEE Transactions on Industry Applications***, vol. 55, no. 3, pp. 2845–2857, May 2019.

[15] J. C. Mayo-Maldonado, J. E. Valdez-Resendiz, P. M. Garcia-Vite, J. C. Rosas-Caro, M. D. R. Rivera-Espinosa, and A. Valderrabano-Gonzalez, "Quadratic buck-boost converter with zero output voltage ripple at a selectable operating point," ***IEEE Transactions on Industry***

Applications, vol. 55, no. 3, pp. 2813–2822, May 2019.

[16] N. Zhang, G. Zhang, K. W. See, and B. Zhang, "A single-switch quadratic buck-boost converter with continuous input port current and continuous output port current," ***IEEE Transactions on Power Electronics***, vol. 33, no. 5, pp. 4157–4166, May 2018.

[17] Neethu Joy, Ninu Joy, and Kavitha Issac, "Dual output switched inductor double switch converter," ***Materials Today: Proceedings***, vol. 58, part 1, pp. 428–432, Mar. 2017.

[18] Sreekutty Shibu, Emmanuel Babu, S. Neema, and Ninu Joy, "High gain DC-DC converter with low voltage stress," ***Materials Today: Proceedings***, vol. 58, part 1, pp. 428–432, Mar. 2018.

[19] Aiswarya P, Beena M Varghese, Ninu Joy, and Anu George, "Switched inductor based bidirectional DC-DC converter for high voltage gain," ***Materials Today: Proceedings***, vol. 58, part 1, pp. 569–576, Mar. 2017.

[20] Saflana N. A., Smitha Paulose, Neetha John, Neema S., and Ninu Joy, "Dual output common ground quadratic boost converter with low duty ratio," ***International Journal of Creative Research Thoughts***, vol. 10, no. 10, Oct. 2017.