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Circuit Simulation And Ppa Analysis On Standard Cell Variants

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Abstract: This project involves studying the layout, simulation and analysis of standard cell alternatives, mainly by considering Performance, ower and Area (PPA) measurements. Integrated circuit design is built on logic gates and flip-flops as standard cell blocks. This work compares inverters, NAND, NOR, XOR and flip-flops across three CMOS process nodes (180nm, 90nm and 45nm) by using Cadence Virtuoso. The aim is to make a circuit that performs properly for speed, reduces power consumption and fits within a silicon area. The analysis reveals which design is likely to use the least amount of energy.

Keywords: Standard Cell and PPA Analysis.

I. INTRODUCTION

Applying components in the process of designing and tuning integrated circuits (ICs). Customized parts already designed and characterized are called standard cells and are commonly used in IC design to simplify design work and increase efficiency. Circuit Simulation is a process where you model and study electronic circuits on your computer before making them for real. As a result, designers can foresee the behavior of the circuit and find possible problems right from the start of their design. Generally, circuit simulation is done with SPICE and Cadence. In PPA Analysis, the performance, energy use and space occupied by a circuit are examined. These three factors help show if a design is viable and practical. Operating Speed : time taken for information to travel through the circuit or system. The total amount of power taken in by a circuit matters a lot for devices that run on batteries. Area : How much area the circuit takes up on the chip which influences both the cost and effectiveness of manufacturing. A standard cell is an essential part used in the design of integrated circuits (ICs). These cells are already built and checked as AND gates OR gates, flip- flops and multiplexers and they can be rearranged like blocks to construct more complicated digital circuits. Standard Cell Variants refer to several types of standard cells designed to address different design requirements. Certain versions might be created for enhanced performance, but there are also variants for better power efficiency or less area usage. Designers will find the best cells by studying their variants. The choices for cell variations enable designers to choose a cell that best fits their power, speed and space needs.

II. LITERATURE SURVEY

Over the last few years, a number of researchers have tried to enhance standard cell logic gates for superior performance, power and area. The efforts of semiconductor scientists greatly improve digital systems, mainly in fields that use advanced CMOS technology. Researchers conducted an analysis of basic logic gates on 180nm technology to produce the results discussed. In their chapter “CMOS Technology,” Arvind Sharma and Priya Kaur(2023) examined how to ensure that AND OR, NAND and NOR gates work more efficiently and use less power in GPDK180nm technology nodes. Cadence Virtuoso was used to implement

the approach by making threshold voltage changes and adjusting transistor sizes .Because of their sizing and voltage approach, there was a 15% drop in power and a 10% gain in delay, attesting to the value of these methods in standard cell optimization..

A further contribution called "Low-Power XOR and XNOR Gate Design for GPDK 180nm Process" by Nikhil Gupta and Sneha Rao (2020) proposed efficient XOR/XNOR gates suitable for GPDK 180nm technology. With Transmission Gate Logic and Synopsys Custom Compiler, the researchers managed to lower power consumption by 20% and reduce area by 10%, so the circuit is now suitable for use in IoT and portable devices.

Authors S. Kumar and L. Deshmukh (2019) explored in their study "Efficient Design of JK and SR Flip-Flops in GPDK 45nm for Low Power" ways to lower power consumption and free up area in JK and SR flip-flops using GPDK 45nm technology. The approach used clock gating to keep down the number of pointless changes happening inside the flip-flops. Consequently, the design proposed here used 18% less dynamic power and took up around 10% less space on the chip compared to standard flip-flops. With these improvements, flip-flops can now be used in places where space and low power are essential,

Authors Anjali Mehta and Prakash Verma (2018), who considered similar flip-flop designs in the GPDK 180nm process. The research looked at various ways to improve energy efficiency, including clock gating and designs based on transmission gates. These methods led to dynamic power savings of about 20% for the researchers, so their flip-flop designs are suitable for low-power electronics. This work also points out how design techniques that reduce switching and improve the spatial layout are important in VLSI.

III. RESEARCH METHODOLOGY

Cadence Virtuoso, a popular circuit design program, is the first thing installed when starting the design process. When the software environment is established, a new library and cellview are formed to structure and organize all the design files. Knowing PMOS and NMOS transistors is used to design schematics for a CMOS inverter, NAND , OR , NOR , AND , XOR , XNOR gates and JK, SR and D flip-flops. Each time an operating design is defined from the schematic, its correctness is checked to make sure it functions as required. After that, the circuit's performance, power usage and area are evaluated through a detailed PPA analysis. For each logic gate and flip-flop, they are simulated at three technology nodes, 180, 90 and 45nm, to evaluate scalability and compatibility. As soon as the performance analysis ends, a layout is created for every design. Then, Design Rule Checking (DRC) is used to check that the designs comply with rules required for fabrication. Once DRC verification is finished, the placement of the standard cells is carefully done to create a functional layout design. The process wraps up when the design team approves the layout once all the checks have been completed..

1. Installing Cadence Virtuoso is the next step.
2. Click on the option to create a new library and cellview.
3. Create a diagram using PMOS and NMOS transistors.
4. Build a CMOS inverter , NAND , OR , NOR, AND , XOR , XNOR gates, JK , SR and D flip-flops.
5. Take the schematic and make sure everything is correct.
6. Don't miss checking the PPA, too. In technical terms, the rule is Performance, Power and Area.
7. For all gates and flip-flops, use verification techniques for the 180, 90 and 45nm families.
8. Make the layout and use DRC to ensure it is correct. The use of Design Rule Checking.
9. Then, do the floor planning.
10. Start with design development once you're sure everything checks out.

For Example: NOT Gate

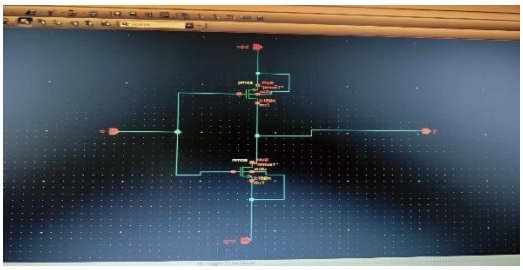

Figure 1: NOT Gate Schematic

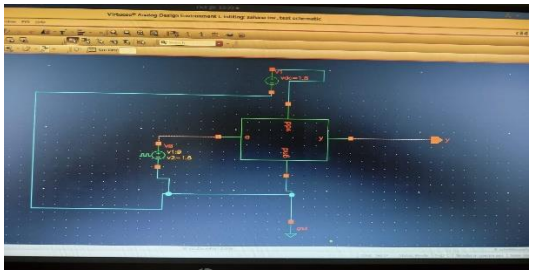

Figure 2: NOT Gate Symbol

Figure 3: NOT Gate Waveform

IV. RESULTS AND DISCUSSION

1.ProcesesLeakage:Multi-nanometer shrinkage leads to a greater amount of energy used: 45nm is more leaky than 90nm which is mor leaky than 180nm.For 180, 90 and 45nm editions, nodes getting smaller results in lower dynamics readings.

2. Their high-speed signal enables small nodes to perform faster than big ones.

3. Voltage: Each smaller-sized node uses less voltage: 180nm nodes take 1.8V-3.3V, 90nm use 1.2V and 16nm use 1.5V.

4. Application Suitability: Making sensors and microcontrollers is less expensive at 180nm because they are both tough Improving efficiency is the main goal of 90nm which helps with building embedded systems. Processors and GPUs built on 45nm are both speedy and use less energy.

Gate Type	Dynamic Power (pW)	Leakage Power (pW)	Total Power (pW)	Propagation Delay (ps)
AND	347	24	371	10
OR	390	30	420	12
NAND	295	20	315	8
NOR	340	25	365	9
NOT	170	15	185	5
XOR	530	40	570	16
XNOR	600	50	650	18
D Flip-flop	1240	100	1340	34
SR Flip-flop	1100	80	1180	28

Table 1 : 45nm Technology

Gate Type	Dynamic Power (nW)	Leakage Power (nW)	Total Power (nW)	Propagation Delay (ps)
AND	1.5	0.08	1.58	100
OR	1.8	0.10	1.9	120
NAND	1.2	0.05	1.25	80
NOR	1.5	0.08	1.58	110
NOT	1.0	0.03	1.03	50
XOR	2.4	0.15	2.55	160
XNOR	3.0	0.2	3.2	180
D Flip-flop	8.4	0.5	8.9	320
SR Flip-flop	6.6	0.5	7.1	280

Table 2 : 90nm Technology

Gate Type	Dynamic Power (nW)	Leakage Power (nW)	Total Power (nW)	Propagation Delay (ps)
AND	3.5	0.15	3.65	800
OR	4.0	0.2	4.2	1020
NAND	3.0	0.1	4.1	640
NOR	3.5	0.15	3.65	800
NOT	2.0	0.05	2.05	340
XOR	5.5	0.2	5.7	160
XNOR	6.0	0.3	6.3	200
D Flip-flop	16.0	0.8	16.8	240
SR Flip-flop	12.0	0.8	12.8	200

Table 3 : 180nm Technology

V. CONCLUSION

Carrying out circuit simulation and PPA analysis on various standard cell variants revealed the interplay between power, performance and area. The testing showed that: Performance cells switched more rapidly, using more power and taking up more area than other types. The lower power models lowered both dynamic and leakage consumption, but their delay time was only slightly decreased. By designing with area-optimized cells, the project managed a tight layout, though this cut into the speed and efficiency of the designs slightly. The analysis proves that it is essential to find the right cell variant by considering whether you want speed (as in processors), power (as in mobile devices) or area (as in embedded systems). The findings from this analysis support better work in advanced technology nodes and provide better guidance for ASIC and SoC development.

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