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Design And Analysis Of 2ghz Phase Frequency Detector Using 45nm Technology

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Abstract— This paper represents the design and analysis of a high-speed Phase Frequency Detector (PFD) working at 2GHz, a component in phase-locked loops (PLLs) used for high frequency bandwidth and synchronization. During simulations, important design factors such as logic gates, delays, reset methods and power usage are examined. The performance is evaluated under various input conditions to check the circuit's reliability and efficiency at GHz frequencies, making it suitable for high-speed communication and processor systems. PFD reduces jitter effect on PLL and enhances the performance of PLL by increasing the locking range and reducing the power consumption. The design is implemented using CMOS technology, ensuring compatibility with modern integrated circuit fabrication processes for compact and power-efficient integration.

Index Terms—PFD, PLL CMOS Logics and Rise time, Fall time, Jitter and frequency

I. INTRODUCTION

CMOS technology is the type of semiconductor technology currently used to produce transistors in modern electronic devices. Today, it is a significant breakthrough for electronic designers to be able to combine all components of a system onto a single chip. As digital and communication systems rapidly advance, accurate timing and synchronization have become essential requirements in system design. Phase-Locked Loops (PLLs) play a vital role in clock generation, data recovery, and frequency synthesis across a wide range of applications including wireless communications, microprocessors, and mixed-signal systems. Phase Frequency Detectors (PFDs) are fundamental components in PLL. The performance of a PLL heavily depends on the accuracy, speed, and reliability of its PFD. In the design of PFD both analog and digital signal are used, different logics are applied in the design. The knowledge of signals makes the PFD more synthesized, challenging environment.

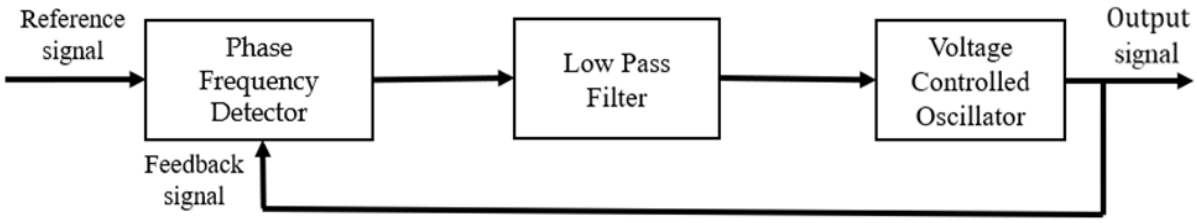

Figure 1: Phase Locked Loop

Figure 1 shows A typical PLL consists of several fundamental components: a Phase Frequency Detector (PFD), a Low-Pass Filter (LPF), a Voltage-Controlled Oscillator (VCO), and often a Frequency Divider in the feedback. This project focuses on the design and analysis of a 2GHz PFD using CMOS technology, aiming for low power consumption, and reliable high-speed performance for modern PLL applications. There are two PD's 1. XOR PD 2. PFD

II. LITERATURE SURVEY

S. Dutta, M. Kumar, and N.Jaiswal [1] examined a range of Phase-Locked Loop (PLL) architectures, organizing them according to their underlying concepts and specific uses. Their study provides valuable insights into how PLL systems have developed and diversified over time.

D. Ray, A. Dutta, and R. Roy [2] introduced an ultra-low-power integrating sub-sampling PLL that functions within the 100–250 MHz range. Their approach removes gain stages, which helps minimize noise injection while maintaining a small footprint and low power usage.

K. Saw and H. S. Singh [3] proposed a charge pump design optimized for power efficiency in fast-locking PLLs. Their configuration aims to reduce power usage while enabling quick phase acquisition.

W. Xu and A. Patel [4] developed a charge pump circuit incorporating a core pump and operational amplifiers, aimed at minimizing current mismatch and lowering phase noise in PLL systems.
J. Ji, T. Zhang, and H. Liu [5] introduced an innovative charge pump design that significantly reduces current mismatch and variation, enhancing the stability and precision of PLL systems.

R. Kumar and P. Singh [6] presented a high-speed CMOS charge pump designed using 90 nm technology for use in PLLs. Operating at 1 GHz with a low supply voltage, the design showcases its effectiveness in high-frequency, low-power applications.

III. XOR PHASE DETECTOR

An XOR phase detector is a digital circuit that compares two input signals—Reference (A) and Feedback (B). It uses an XOR gate to generate an output pulse, where the duty cycle of the pulse reflects the phase difference between the two inputs. If the input signals are exactly in phase, the XOR gate output stays at 0, meaning there's no phase difference. As the phase shift between the signals increases, the XOR output produces wider pulses, showing a larger phase error. This pulse width acts as an indicator of the timing difference and can be used in a PLL system to correct it. Because it's simple, fast, and easy to implement, the XOR gate is a popular choice for digital phase detection in high-speed systems.

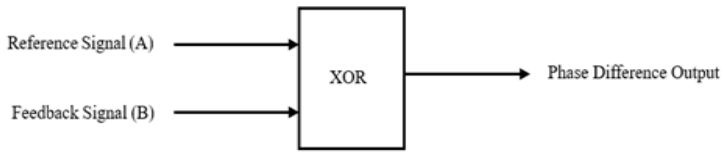

Figure 2: XOR PD

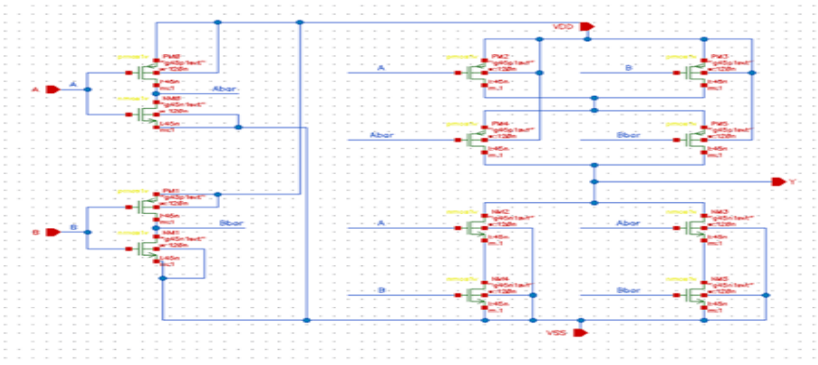

Figure 3: Schematic of XOR PD

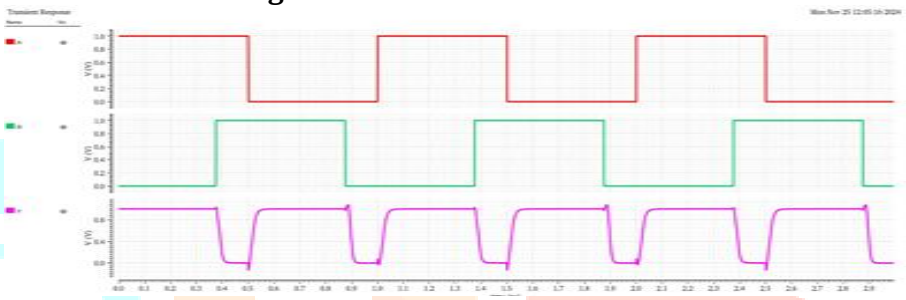

Figure 4: Same frequency, 135 degree phase shift of B

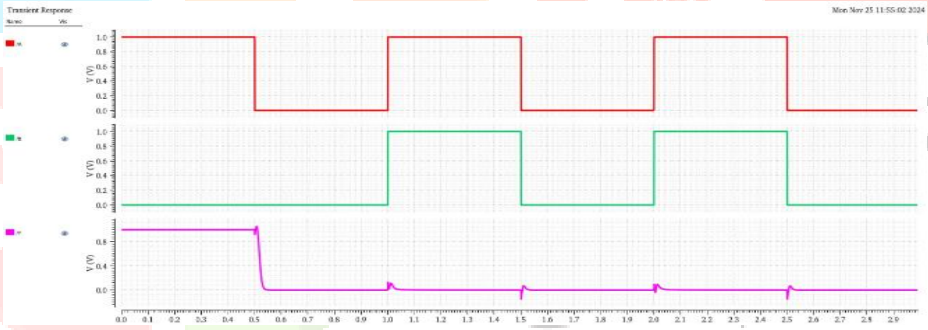

Figure 5: Same frequency, 360 degree phase shift of B

The XOR phase detector has a major limitation it can measure how much two signals are out of phase but can't tell which one comes first. It also can't detect phase shifts irrespective of limits, which makes isn't suitable for systems that need complete, it works best with clear, evenly shaped signals (like perfect square waves with a 50% duty cycle). If the input signals are noisy or uneven, the detector may give incorrect results or not work properly.

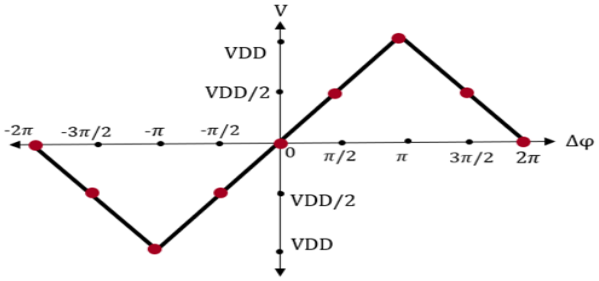

Figure 6: I/O Characteristics of CMOS XOR phase detector

The XOR phase detector produces an output voltage that forms a pattern which is triangular which in response to the phase difference between its two inputs. As the phase shift increases from (0° to 180°), the output voltage rises from 0 to its maximum value (VDD). As the phase continues from (180° to 360°), the voltage then falls back to zero. Since the output pattern repeats, it causes confusion—phase differences such as 90°

and 270° produce the same voltage. This limits the detector's ability to accurately measure phase shifts beyond 180°.Also, the XOR detector can't detect changes in frequency, it only works correctly when both input signals share the same frequency. Due to these drawbacks, XOR detectors are not ideal for or reliable to use in Phase-Locked Loop (PLL) systems.

Because of the drawbacks, modern PLLs use PFDs, which can measure both phase and frequency differences over the entire 360° range and also indicate which signal is leading or lagging and optimize the lock time and stability in PLL.

IV. PHASE FREQUENCY DETECTOR

A Phase-Frequency Detector (PFD) is built using resettable D Flip-Flops (DFFs) along with a reset circuit. These DFFs capture the rising edges of the input signals to detect both phase and frequency differences, while the reset logic ensures that the outputs don't overlap, allowing for precise and reliable operation.

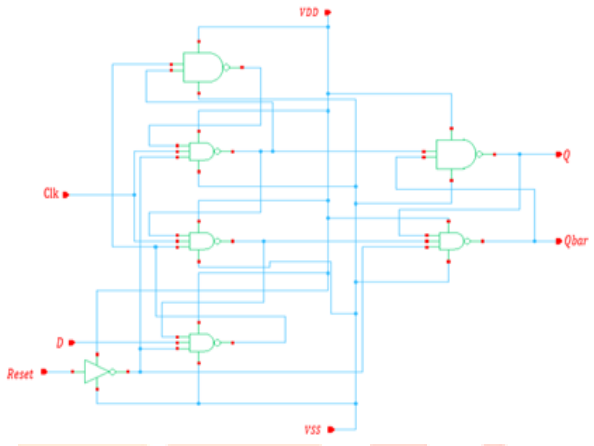

Figure 7: Schematic of Resettable DFF

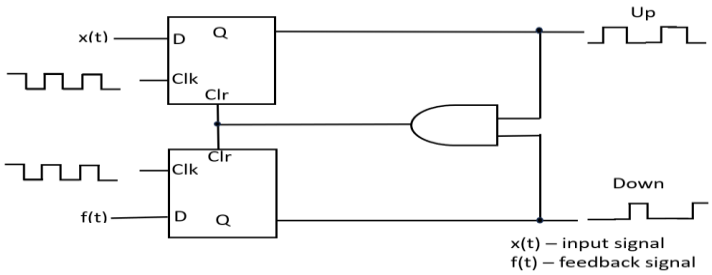

Figure 8: Phase Frequency Detector

A Phase-Frequency Detector (PFD) is a key component in modern Phase-Locked Loops (PLLs), designed to compare both the phase and frequency of two input signals—typically a reference clock and a feedback signal. It generates two outputs that indicate whether the feedback signal is leading or lagging the reference, providing magnitude and direction. This directional capability allows the PLL to adjust more accurately and lock faster. PFD operates reliably across the full 360° phase range and handles varying duty cycles effectively. Its main function is to detect any difference in phase or frequency between the two signals and generate corresponding output signals (usually UP and DOWN) that guide the control elements of the PLL. The PFD outputs an UP signal when the reference clock leads, and a DOWN signal when the feedback clock leads. These outputs are then used to adjust the VCO to match the reference clock. It also helps eliminate the dead zone problem common in simpler detectors, has fast response time, and ensures accurate phase alignment with low jitter. It is critical for applications like high-speed data communication, clock recovery, and frequency synthesis.

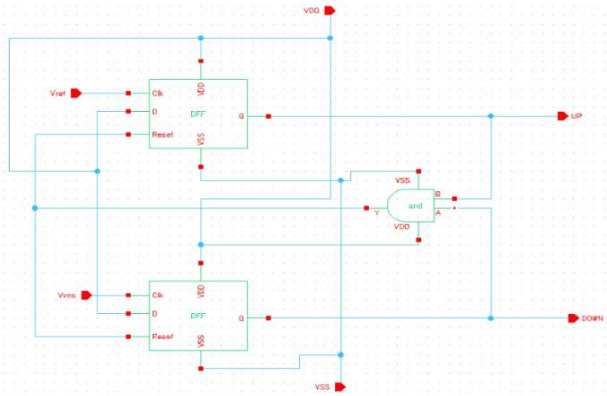

Figure 9: Schematic of PFD

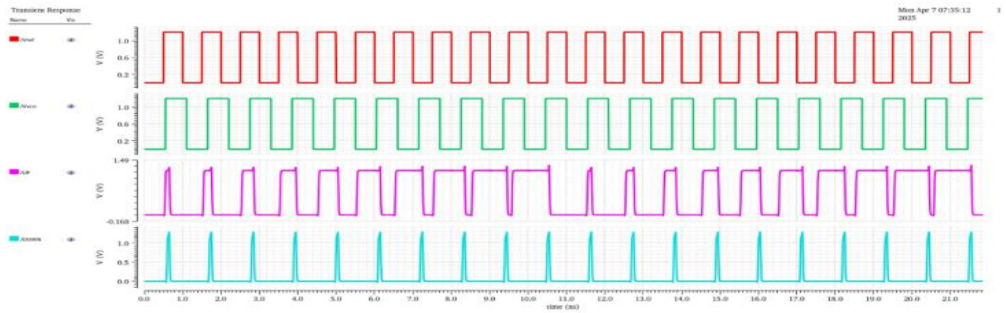

Figure 10: fvco 900MHz

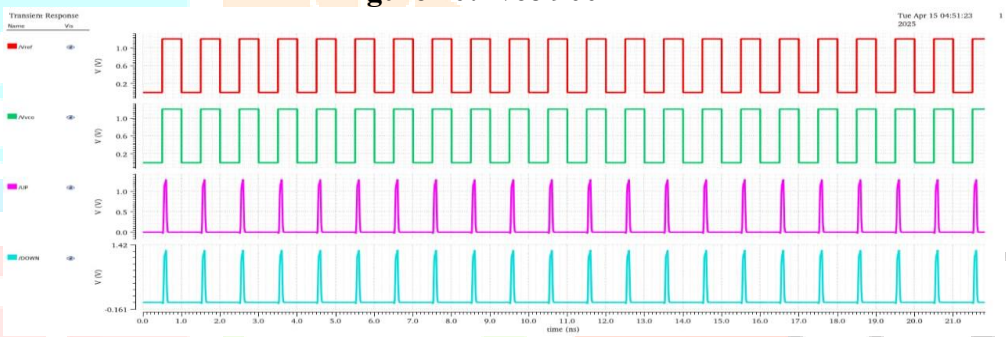

Figure 11: fvco 1GHz

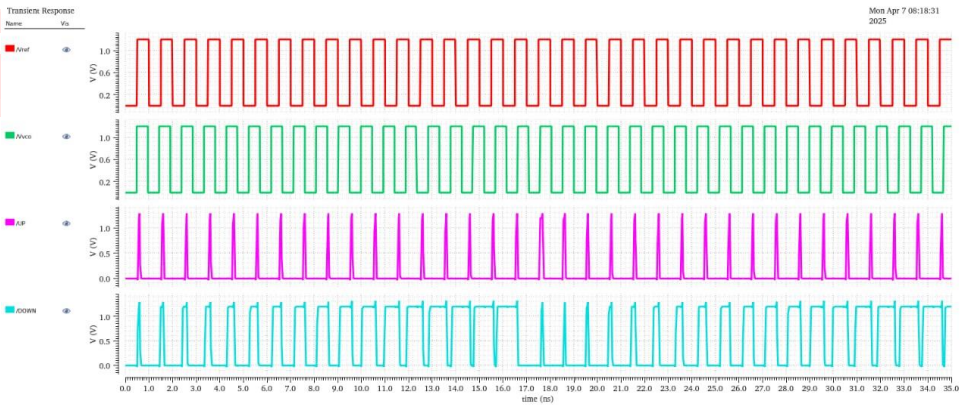

Figure 12: fvco 1.1GHz

V. PROBLEM STATEMENT

Traditional XOR phase detectors are limited by their inability to detect phase direction and operate beyond 180°, making them unsuitable for high-frequency applications. This project addresses the design challenges of a 2GHz Phase-Frequency Detector (PFD), focusing on minimizing dead zone, ensuring fast and accurate detection, and achieving reliable performance for modern high-speed PLL systems.

VI. OBJECTIVES

- To design XOR PD and observe its limitation so, further design 1GHz Phase Frequency Detector using 45nm technology in Cadence.
- We use a PFD over an XOR Phase Detector.
- As XOR Phase Detector limits the phase difference only up to 90 degrees

VII. PROPOSED METHODOLOGY

1. The PFD detects the rising edges of both the input and feedback signals.
2. If the input signal rises before the feedback, the "Up" signal is activated and "Down" stays low.
3. If the feedback signal rises first, "Down" goes high while "Up" remains low.

VIII. RESULT AND WORKING MODEL

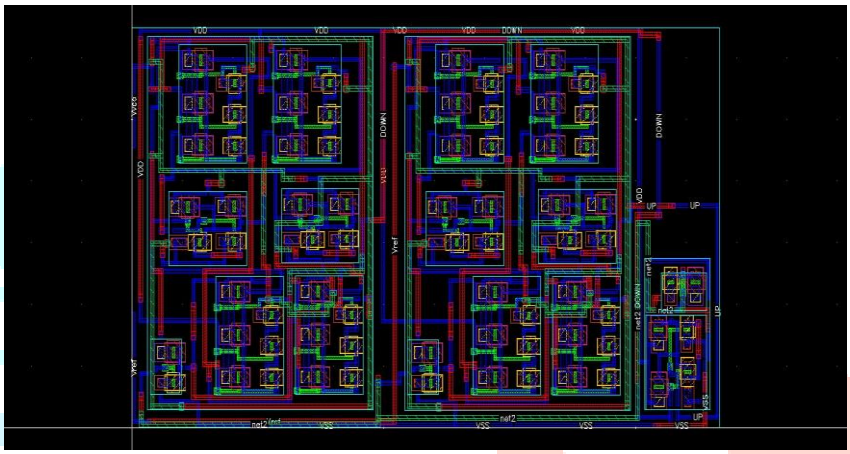

Figure 13: Layout of PFD

IX. CONCLUSION

Designed and simulated a 2GHz Frequency Detector, focusing on both the circuit and layout design aspects. Through careful simulation, we ensured the detector met the required performance criteria for accurate frequency detection at 2GHz. The detailed layout was created with consideration enhancing the overall reliability and functionality of the design.

Furthermore, the design verification was completed by performing Design Rule Check (DRC) and Layout Versus Schematic (LVS) tests, confirming that the layout adhered to fabrication constraints and matched the intended circuit schematic. These verification steps validated the integrity and manufacturability of the design, ensuring that the frequency detector is ready for further stages such as fabrication or integration into larger systems.

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