IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Comparative Analysis Of 32-Bit Carry Look Ahead Adder Using Ecrl And Pfal Logic

[1]Shaik Hibza, [2] C.Padma

[1] M.Tech Scholar , [2] Associate Professor,

[1,2] Department Of ECE,

[1,2] Sri Venkateswara college of Engineering, Tirupati, Andhrapradesh, India

Abstract: Adders are digital circuits used in VLSI (Very Large Scale Integration) architecture that carry out arithmetic operations, particularly addition, on binary values. They are employed in a wide range of devices, such as memory systems, digital signal processors, and microprocessors. Logic gates that accept two binary values as inputs and output a binary sum make up an adder. These days, designing low power VLSI circuits heavily relies on low power circuits. Adiabatic circuits explain reversible logic, or the reuse of the same, which results in power savings. Using the traditional approach, CMOS circuits are utilized to lower circuit power dissipation. A number of adiabatic techniques were developed to address the shortcomings of CMOS circuits. These techniques use charging and discharging to further reduce power dissipation. Efficient Charge Recovery Logic.

Index Terms - Carry Look Ahead Adder (CLA), Half Adder Circuit, Full Adder Circuit, Efficient Charge Recover Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL).

I. INTRODUCTION

Adders are digital circuits used in VLSI (Very Large Scale Integration) architecture that carry out arithmetic operations particularly addition, on binary values. They are employed in a wide range of devices, such as memory systems, digital signal processors, and microprocessors. Logic gates that accept two binary values as inputs and output a binary sum make up an adder. A half adder, the most basic type of adder, can only generate a sum of 0 or 1, but it can add two single binary digits. In contrast, a full-adder can generate a sum of 0, 1, or 2 by adding three binary digits (two inputs plus a carry from an earlier addition). However, a full-adder needs extra logic to manage the carry—the value carried over from one addition to the next—because binary numbers only employ 0 and 1 [1].They include carry select adders, carry skip adders, carry look forward adders, and ripple carry adders. They differ in terms of performance, area, and power consumption tradeoffs. One example is straightforward, however using ripple carry adders to add big numbers necessitates numerous steps, yet they have a slow propagation delay, making it unsuitable for applications requiring high frequencies. Carry-look ahead adders, on the other hand, need more sophisticated circuitry and use more power, but they have fewer stages in which to add big numbers [2]. Distinct features and compromises with regard to power consumption, space, and performance [3]. For instance, ripple-carry adders require many stages to add large numbers and have a slow propagation delay, despite being straightforward and quick to design. Conversely, carry look ahead adders need more complicated circuitry and use more power, but they may add big numbers with fewer stages [4]. The performance and efficiency of adders are crucial elements in the operation of digital systems, and they are a key component in VLSI design. This thesis' primary goal is to offer Very Large Scale Integration (VLSI) designers more low power options. In particular, this work focuses on reducing power dissipation, which is growing steadily as technologies are scaled down. Several methods have been used at various stages of the design process to lower power dissipation at the system, architectural, and circuit levels.

To overcome these difficulties, a number of power optimization strategies have been created, such as clock gating, power gating, and dynamic voltage and frequency scaling (DVFS). By reducing energy dissipation through progressive voltage transitions and energy recovery, adiabatic logic presents a promising approach among new low-power design techniques [5]. In contrast to traditional CMOS logic, which uses a lot of power during quick cycles of charging and discharging, adiabatic circuits recycle energy using reversible computing concepts, which lowers total power loss. Beyond 2030, advancements in semiconductor technology like Intel's Power Via technology and Backside Power Delivery (BPD) are intended to improve performance and power efficiency. Furthermore, the widespread use of machine learning and artificial intelligence (AI) models has raised the demand for computing power, making additional improvements in integrated circuit power efficiency necessary to support future technological development. optimization strategies as the semiconductor industry works within the bounds of Moore's Law. Adiabatic logic and new power delivery techniques offer a feasible option to achieve significant energy efficiency gains, guaranteeing long-term advancements in VLSI technology.

II. LITERATURE SURVEY

New ECRL-CMOS interface circuit with low power consumption, Morell, W. and Srivastav [1], A. IEEE's 62nd 2019's Midwest Symposium on Circuits and Systems (MWSCAS) In this paper, a unique interface circuit for integrating ordinary CMOS logic with Efficient Charge Recovery Logic (ECRL) is shown. By reusing energy during switching events, ECRL, a type of adiabatic logic, lowers power dissipation. However, effective interfacing is still a significant difficulty because ECRL and CMOS have intrinsically different signal patterns and timing. Vol. 5, No. 1, pp. 1213–1218, 2019; The International Journal of Advance Research and Innovative Ideas in Education Adiabatic Logic for Power Recycling Using Low Power ECRL P. V. Kumar[2] et al. The study looks into using an adiabatic logic type called Efficient Charge Recovery Logic (ECRL) to lower dynamic power consumption in CMOS devices. By recycling charge during switching activities and using a power-clock supply for controlled charging/discharging, the work aims to increase energy efficiency.

A crucial component of distributed and ubiquitous computing systems is addressed in the study by Enokido [3] et al. (2011): reducing overall power usage through control of both processing and transmission speeds. Energy efficiency is a major challenge in wireless and mobile networks because of the need for sustainable operation and the restricted battery capacity. Urban transit systems are critical for sustainable urban development. However, designing an efficient public transportation network involves solving multiple complex sub-problems including transit network design (TND), frequency setting, and fleet size calculation, which are inherently NP-hard due to the numerous variables and constraints involved. In the 2023 study by Jiménez- Carrión[4] et al., the The authors describe a multi-objective optimization strategy that makes use of genetic algorithms. (GAs) to address these transit planning challenges simultaneously. Their model seeks to minimize user travel time and operator costs while maximizing service quality and coverage.

In 2024, 2024, Pierre Vandergheynst, David Atienza, Nadia Khaled, and Hossein Mamaghanian presented a novel method for processing ECG signals using compressed sensing (CS) that was specifically designed for wireless body sensor nodes. Energy-efficient wearable sensors that can continually evaluate cardiovascular health are made possible by this discovery, which is crucial for Internet of Things-based health monitoring[5].This groundbreaking work lays the groundwork for future AI-driven ECG analysis and predictive healthcare analytics, although not explicitly relying on AI. Malhotra [6] et al. (2019) concentrate on designing a low-power 4:2 compressor with power gating approaches and ECRL-based adiabatic logic. A 4:2 compressor is an essential part of accumulators and multipliers, which are frequently seen in arithmetic and DSP circuits. High switching activity and power dissipation are problems for conventional CMOS-based compressors, particularly at higher frequencies.

The application of circuits using Positive Feedback Adiabatic Logic (PFAL) for low-power digital design is investigated by Indumathi [7] (2018). By recycling charge utilizing the concepts of reversible computing, PFAL, a kind of adiabatic logic, is well-known for lowering energy dissipation during switching events. The design of PFAL-based circuits, which provide significant power savings over traditional CMOS logic, is the main topic of the article. article. Complementary Pass, Complementary Metal-Oxide-Semiconductor (CMOS) CPL, or transistor logic and Differential Pass Transistor Logic (DPL) are three different logic styles that are compared in the implementation of arithmetic circuits, specifically different types of adders, including ripple carry adders, half adders, and full adders, in the study by Nagaraj [8] et al. (2017).

An Efficient Charge Recovery Logic (ECRL) circuit is described by Moon and Jeong [9] in their 1996 publication that uses adiabatic switching approaches to lower dynamic power consumption in digital VLSI systems. The inherent energy inefficiencies in conventional CMOS logic, where a large amount of Power is lost as the load is being charged and discharged capacitances, are addressed in this work, which is fundamental to the creation of adiabatic logic families. Charge recovery logic (CRL) has become a potential method for attaining energy-efficient operation in VLSI systems as the need for digital circuits with high speed and low power keeps growing. A revolutionary high-speed charge recovery logic (CRL) design that can operate at 1.6 Gb/s is shown in the work by Yu, Chiu, and Kuo [10] (2010). This design is intended for applications that need high throughput and power efficiency.

Zheng, Y., Xu, R., & Wang, X. [11]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(12), 2535–2544, "An energy-efficient 10 Gb/s charge recovery logic with high linearity and low power usage," a quick, low-power charge recovery logic circuit with a 10 Gb/s operating speed is presented in this study. [12] Roy, K., Kim, S. W., and Kim, H. S. (2006). Dynamic voltage scaling in a high-speed charge recovery logic circuit. 904–910 in Solid-State Circuits Journal, IEEE 41(4). In order to increase power economy without sacrificing performance, this work introduces a high-speed charge recovery logic (CRL) circuit that incorporates dynamic voltage scaling (DVS). The authors discuss the common trade-off that charge recovery logic designs face between speed and energy usage.

By using Charge Recovery Logic (CRL), Kang et al. [13] offer a novel method for obtaining both high speed and low power consumption in serial data communication. The design and implementation of a Charge Recovery Flip-Flop (CRFF) and its incorporation into a serial link transceiver, optimizing it for energy efficiency, constitute the paper's primary contribution. The authors present an adiabatic structure based on differential logic that takes advantage of energy recovery in the cycles of charging and discharging. Using adiabatic switching approaches, Sridhar and Kang (2002) [14] proposed a high-efficiency charge recovery logic (CRL) circuit with the goal of lowering dynamic power consumption. By effectively recovering charge from the load capacitance during the discharge phase, the scientists aimed to reduce energy loss.

Mukherjee and Roy (2010) [15] introduce Asynchronous Adiabatic Logic (AAL), a revolutionary method for lowering energy consumption in digital circuitry. This technique, in contrast to conventional synchronous adiabatic logic, does not require a global clock, which lowers power overhead and increases energy efficiency, particularly in ultra-low power applications. The suggested architecture makes use of adiabatic switching concepts, which recover and reuse charge to minimize the energy lost during logic transitions. P. Balasubramanian et.al [16] proposed new carry look ahead adder by using with hold look-ahead adder modules of varying sizes.The proposed design is implemented in convention CMOS 28nm CMOS standard cell for reduction of power consumption here the author proposed kogge-stone adder.

The work is driven by the growing need for low-power and high-speed VLSI architectures, particularly in embedded and portable devices. The study uses modeling tools and standardized 180 nm CMOS technology to assess the adders power-delay product (PDP), propagation delay, and power usage. The development and optimization of a hybrid PTL-PFAL circuit framework that reduces area, boosts power efficiency, and improves delay performance in VLSI systems is the main goal of this study. This study aims to assess the benefits of integrating PTL into PFAL, guaranteeing robust signal integrity and energy-efficient logic circuits. VLSI circuits use adiabatic logic, a low-power design method. By lowering energy dissipation, it provides notable power savings. Positive Feedback in this Paper Studies have shown that PFAL-based designs can achieve up to 90% energy savings over traditional CMOS implementations, making PFAL a potential option for safe and energy-efficient hardware solutions. For this reason, the adiabatic logic style was chosen from the literature. However, it also presents a number of difficulties. [17-21] discussed about various adders as CLA, CSA, Vedic Adder and Approximate Adders.

III. PREVIOUS WORK

Power Management Circuit Design Uses The Efficient Charge Recovery Logic (Ecrl) Approach Of Electrical Gadgets [6, 7]. The Purpose Of The Implementation Is To Extend The Battery Life And Power Management Circuitry Efficiency Of Portable Electronic Devices [8, 9]. During The Power Management Process, Ecrl Recovers Power From Charges That Would Otherwise Be Lost. When A Power Management Circuit Uses A Battery To Power A Gadget, Some Energy Is Lost [10**].** Ecrl Takes Advantage Of This Energy Loss, Capturing The Energy And Storing It In A Capacitor For Later Use. The Recovered Charge Can Either Be Kept In The Battery To Extend The Gadget's Lifespan Or Used To Power The Device Directly. Additionally, It Shows That Ecrl Can Be Applied To Enhance The Device's Efficiency By Lowering The Heat

Generated By The Power Management Circuitry [11]. Ecrl Has Historically Been Used In Conjunction With Other Power Management Strategies, Such As Adaptive Voltage Placement, Power Gating, And Voltage Scaling. To Construct A Power Management System That Is Extremely Effective And Efficient [12]**.** When Used Properly, Ecrl Can Significantly Extend Battery Life, Which Is Crucial For Battery-Powered Portable Electronics. When Designing Power Management Circuits For Electronic Devices, Efficient Charge Recovery Logic (Ecrl) Provides The Following Benefits **:**

Enhanced Efficiency: ECRL restores the charge after it is lost due to the power management procedure [13, 14]. As a result, more energy is available for using the device or extending the battery life because less energy is lost during the voltage change.

Longer Battery Life: To increase the battery's lifespan, ECRL can restore and store the charge that has been lost. This is particularly crucial for portable, compact electronics with often short battery lives. While there are a number of positive advantages to using Efficient Charge Recovery Logic (ECRL) in power administration design circuits for electronic devices, there are also some possible drawbacks to take into account:

Complexity: Designing power management circuits becomes more difficult when ECRL is realized since it may call for more circuitry. However, this may complicate circuit design and testing, increasing the time and expense of development.

Larger Circuit: A capacitor is required for stored energy recovery (ECRL) in order to store the recovered energy [15]. When there is limited space, it is important to keep an eye on the power management circuit's size as it may increase.

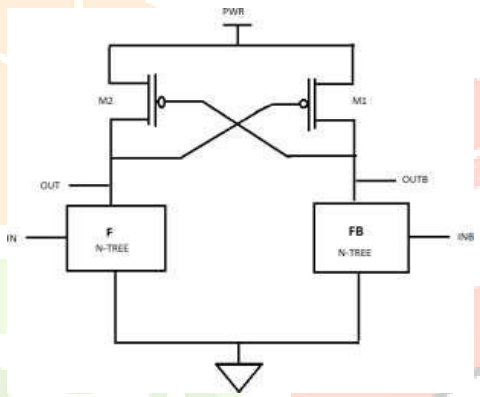

Fig. 1. ECRL

Two cross-coupled PMOS transistors and a functional N block as shown in Fig. 1.The circuit has certain limitations because of its simple partial adiabatic logic design. When the power source is more than threshold value, both cross-coupled PMOS transistors stop the working and resulting in non adiabatic losses.

IV. METHODOLOGY AND IMPLEMENTATION

The effective use of multiply-accumulate (MAC) units in VLSI design is critical for improved computational performance and energy efficiency since they are fundamental to digital signal processing (DSP), machine learning, and high-performance computing. Applications like filtering, convolution, and neural networks are greatly impacted by high-speed MAC units, and devices that run on batteries benefit from efficient designs that lower power usage. However, issues like excessive power consumption, propagation delay, and process variability arise when MAC units are implemented. Performance and dependability in contemporary electronic applications are further improved by utilizing sophisticated multiplier structures, low power methods, and area-efficient strategies.

A. Half Adder

The half adder circuit adds the two input bits and computes the sum and output bits. It is a basic adder circuit. The half adder block diagram is shown in Fig. 2. Present findings include inputs A and B as well as Sum and Carry. If one or both of the inputs are 1, the carry is 1 and the sum is 0. Carry is 0 and total is 1 if both inputs are 1. If both inputs are 0, then both carry and sum are zero. The half adder truth table is displayed in Table I. Fig. 3 illustrates how the Half Adder circuit schematic is implemented with a single XOR and AND gate.

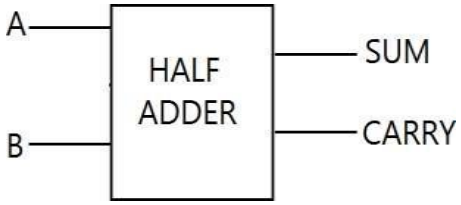

Fig. 2. Half Adder

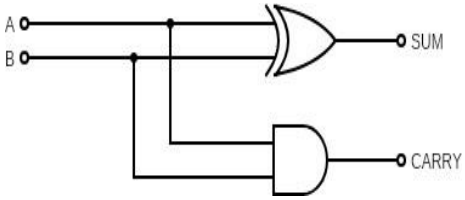

Fig. 3. Half Adder Logic Diagram

TABLE I. HALF ADDER TRUTH TABLE

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

B. Full Adder

A basic arithmetic circuit with three inputs and two outputs—Sum and Carry—is called a complete adder. The full adder block diagram is shown in Fig. 4. The output sum and carry are zero when all of the inputs are zero; the output sum is one and the carry is zero when any one of the inputs is one; the output sum is zero and the carry is one when two of the inputs are one; and the output sum is zero and the carry is one when all three inputs are one. Because only two logic circuits need to be designed, the suggested full adder architecture is easy to understand and uses less space, as seen in Fig. 5. There are two delays since it takes the same amount of time to generate the sum and carry outputs. The full adder design suggested was selected to assess the favored adiabatic logic models in this study due to the aforementioned benefits, as illustrated in Fig. 6. Additionally, Table II offers the whole adder truth table. Three binary single-bit values are added by the Full Adder. The least important portion of the outcome is represented by the Sum output. The most important bit is represented by the carry-out output and is delivered to the subsequent adder step.

Since addition is the most basic operation in digital electronics, the performance of full adders has a direct impact on the processor's overall performance. High-speed, low-power, and area-efficient full adders are necessary for modern VLSI systems.

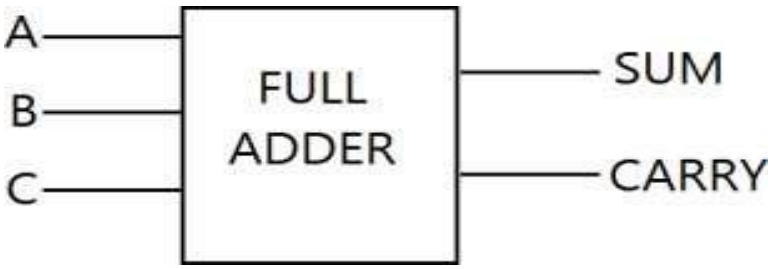

Fig. 3. Full Adder

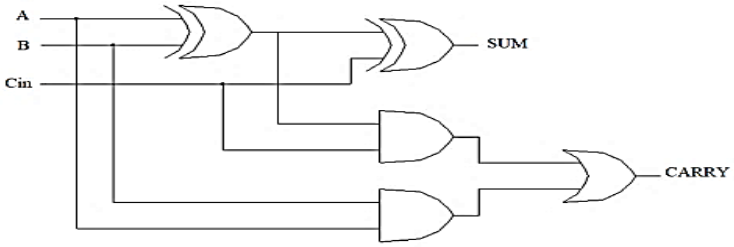

Fig. 5. Full Adder Logic Diagram

TABLE II. FULL ADDER TRUTH TABLE

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

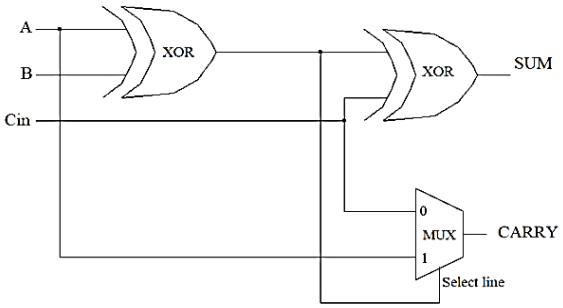

Fig. 6. Proposed Adiabatic Full Adder Design

C. PFAL

Fig.7. illustrates the basic structure of this adiabatic logic style, which was selected because it uses less power than other adiabatic logic families. Because the NMOS functional blocks are linked in parallel to the transmission gates and cross-coupled PMOS transistors.are generated in this design, which is comparable to the 2N-2N2P logic approach. The charging path's equivalent resistance drops as a result of this creation, increasing the logic style's power savings (Narimani, Safaei, and Ejlali 2020). Positive comments In addition to using electricity from the grids, adiabatic logic was first proposed by Vetali in 1996 [12–14] and demonstrates a strong concern for the effective use of electric energy in resolving power-related problems. PFAL is part of the dual rail logic family, which needs Therefore, it is crucial to focus on low availability power and complementary circuits instead of just high performance circuits. Inputs to the logic function that is not complementary.

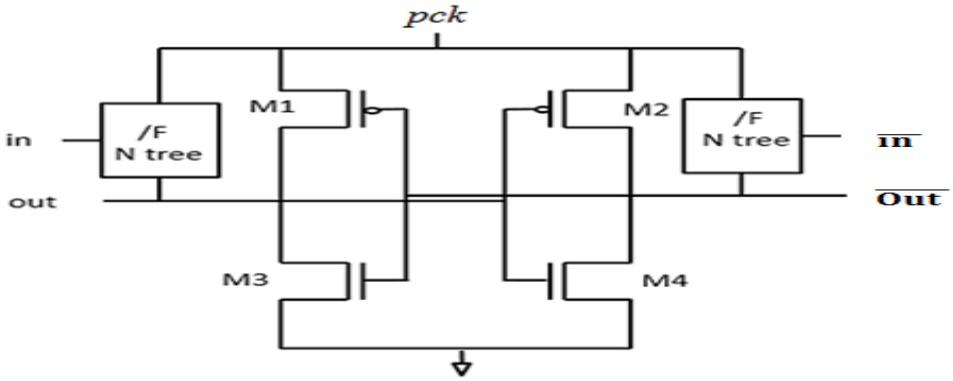

Fig. 7. Basic structure of PFAL logic

A. 32-Bit Adders using PFAL Full Adder Three different types of 32-bit adders are implemented using the PFAL full adder once it is designed:

Carry Adder for Ripples (RCA):

A 32-bit Ripple Carry Adder (RCA) is a sequential arrangement of 32 full adders that performs binary addition on two 32-bit variables. After receiving three inputs—two operand bits and a carry-in—each full adder generates a sum and a carry-out. The main characteristic of an RCA is that the carry-out from each full adder as the carry passes through the chain is the carry-out from each full adder is transmitted as the carry-in to the subsequent full adder, producing a ripple effect. This design's main flaw is the carry propagation delay, which makes it comparatively slow for operations requiring a high bit width and grows linearly with the number of bits. Despite this, the ripple carry adder is appropriate for applications where speed is not a crucial consideration because it is straightforward and effective in terms of hardware implementation.

Carry Save Adder (CSA):

A 32-bit Carry Save Adder (CSA), a fast arithmetic circuit, is utilized to add several binary integers efficiently, especially in big integer addition and multiplication. A CSA lowers the latency by calculating sums and carries independently at each stage without instantly propagating the carry, in contrast to a Ripple Carry Adder (RCA), which propagates carry bits sequentially. It is made up of a number of complete adders, each of which takes three input bits and produces two outputs: a carry bit and a sum bit. The carry bits are saved and moved for the subsequent addition step, while the sum bits create a partial sum. The CSA improves computing speed by drastically lowering the critical route latency as compared to a ripple carry adder because carries are not propagated instantly. The sum and carry vectors must be combined by a final adder, such as a either a Ripple Carry Adder or a Carry Look Ahead Adder, in order to produce the desired outcome. Because of this, the CSA is a crucial component of high-performance arithmetic circuits, particularly those used in computer arithmetic units and digital signal processing.

V. SIMULATION RESULTS

This paper uses the suggested PFAL logic to implement the suggested full adder and the described 32-bit carry look ahead adder.The following Table.III shows the implementation results for different operating frequencies when implemented in tanner tool at 22nm technology results were compared with existing ECRL logic.

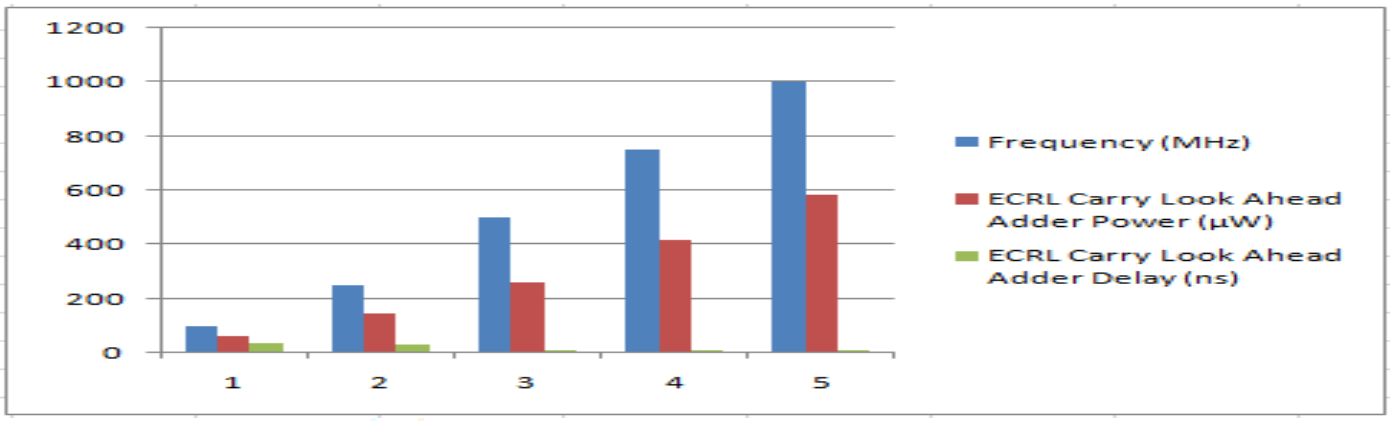

Fig. 8. Simulation Results of 32-bit CLA Adder with ECRL Logic

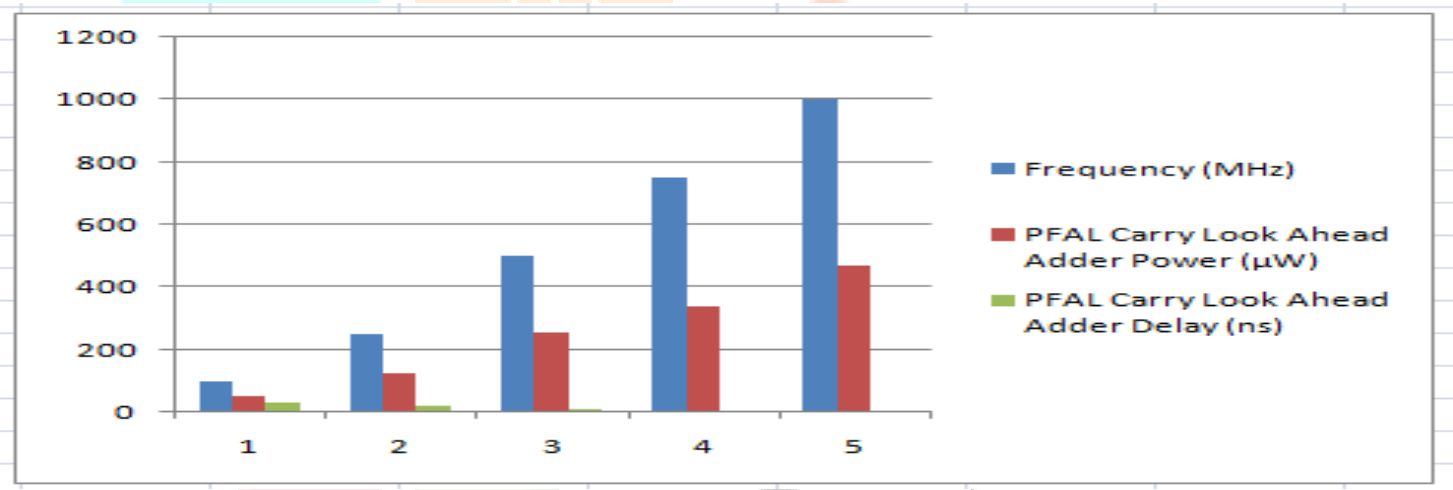

Fig. 9. Simulation Results of 32-bit CLA Adder with PFAL Logic

TABLE III. PERFORMANCE COMPARISON OF 32-BIT ADDERS

Frequency (MHz)	Existing ECRL Carry Look Ahead Adder		Proposed PFAL Carry Look Ahead Adder	
	Power (µW)	Delay (ns)	Power (µW)	Delay (ns)
100	64.90	34.84	50.07	31.34
250	144.74	29.95	124.75	22.07
500	262.05	8.41	255.56	7.93
750	415.97	8.01	341.57	7.68
1000	584.16	8.58	470.88	7.51

The table III provides comparison results of power delay of proposed 32 bit carry look ahead adder with existing ECRL with proposed PFAL logic with different operating frequencies. Compared to existing ECRL Logic the proposed PFAL logic provides better power consumption and decreased delay, hence the performance of 32 bit carry look ahead adder improved interns of power and delay. Figure 8 shows the existing ECRL Logic power, delay values with different operating frequencies. Figure 9 shows the proposed PFAL Logic power, delay values with different operating frequencies.

VI . CONCLUSION

The Proposed PFAL adiabatic logic proposed full adder and 32-bit CLA adder achieve higher speed, lower power consumption, and better energy efficiency compared to traditional ECRL implementation. This makes them the proposed system is well-suited for low-power arithmetic circuits in processors, DSPs, and energy-efficient computing applications. In the proposed research work power consumption will be further decreased by proposed pass transistor logic based full adder using adiabatic technique in future scope to design an efficient 32 bit carry look ahead adder.

REFERENCES

1) W. Morell and A. Srivastava, "Novel, Low-power ECRL-CMOS Interface Circuit," *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, TX, USA, 2019, pp. 25-28, doi: 10.1109/MWSCAS.2019.8885081.
2) P. V. Kumar and P. R. Promodhreddy, "Low Power ECRL Based Adiabatic Logic for Power Recycler," *International Journal Of Advance Research and Innovative Ideas in Education*, Vol.5, Issue no: 1, pp: 1213–1218, 2019.
3) Enokido, T., Aikebaier, A., & Takizawa, M. "Computation and Transmission Rate Based Algorithm for Reducing the Total Power Consumption," Journal of Wireless Mobile Networks, Ubiquitous Computing, and Dependable Applications, volume: 2, number: 2, pp. 1-18, 2011.
4) Miguel Jiménez-Carrión, Gustavo A. "Flores-Fernandez and Alejandro B. Jiménez-Panta Efficient Transit Network Design, Frequency Adjustment, and Fleet Calculation Using Genetic Algorithms," *Journal of Interner Services and Information Security (JISIS)*, vol.13, No.4, November 2023, pp. 26-49 DOI: 10.58346/JISIS. 2023.14.003.
5) K. Bhargava Ram Dinesh, R. Vinoth, and M. V. R. Kashyap, "Design and Implementation of High-Speed 32-bit MAC Unit," *Journal of Physics: Conference Series*, vol. 2571, no. 1, pp. 012027, 2023. doi: 10.1088/1742-6596/2571/1/012027.
6) N. Malhotra, A. Mann and N. Pandey, "Design of Low Power ECRL Based Power Gated 4:2 Compressor," *2019 6th International Conference on Signal Processing and Integrated Networks (SPIN)*, Noida, India, 2019, pp. 891-895, Doi: 10.1109/SPIN.2019.8711712.
7) Amit Saxena1, Deepti Shinghal1, Kshitij Shinghal, "Design and Implementation of Adiabatic based Low Power Logic Circuits," *International Research Journal of Engineering and Technology (IRJET)*, Vol.2, Issue No.2, May 2015.
8) S. Nagaraj, G. M. S. Reddy and S. A. Mastani, "Analysis of different Adders using CMOS, CPL and DPL logic," *2017 14th IEEE India Council International Conference (INDICON)*, Roorkee, India, 2017, pp. 1-6, Doi: 10.1109/INDICON.2017.8487636.
9) Yong Moon and Deog-Kyoon Jeong, "An efficient charge recovery logic circuit," in *IEEE Journal of Solid-State Circuits*, vol. 31, no. 4, pp. 514-522, April 1996, Doi: 10.1109/4.499727.
10) Yu, T.-C., Chiu, C.-T., & Kuo, C.-L. "A 1.6 Gb/s charge recovery logic for low-power and high-speed applications," *IEEE Journal of Solid-State Circuits*. 45(12); pp. 2631–2640, 2010.
11) Wang, X., Zheng, Y., & Xu, R. "An energy efficient 10 Gb/s charge recovery logic with high linearity and low power consumption," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, 22(12); pp. 2535–2544, 2014.
12) K. Roy, S. W. Kim, and H. S. Kim, “Scaling logic circuit for high-speed charge recovery: A dynamic voltage scaling approach,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 904–910, Apr. 2006.
13) Kang, D.-S., Lee, S.-J., & Lee, S.-G. “Design of high-speed and low-power charge recovery logic for serial links,” *IEEE Transactions on Circuits and Systems II: Express Briefs*. 63(6); pp. 547–551, 2016.

14) Sridhar, S., & Kang, S. M. "Design and analysis of a high efficiency charge recovery logic circuit," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems.* 10(6); pp.847–851, 2002.

15) Mukherjee, A., & Roy, K. "Asynchronous adiabatic logic design for ultra-low energy applications," *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*. Pp. 343–348, 2010.

16) P Balasubramanian and Douglas L. Maskell "A New Carry Llook-Ahead Adder Architecture Optimized for Speed and Energy," *Electronics*, 2024, 13(18),3668; https://doi.org/10.3390/electronics13183668.

17) C. Padma, P. Jagadamba, P. Ramana Reddy, "Efficient Cached 64 Point FFT Processor Using Floating Point Arithmetic for OFDM Applications", Instrumentation Measure Metrologies, ISSN:1631-4670, (SCOPUS Indexed) vol. 21, no. 1, pp. 21-26, February 2022. DOI: https://doi.org/10.18280/i2m.210104.

18) C. Padma, P. Jagadamba, P. Ramana Reddy, "Design of FFT Processor Using Low Power Vedic Multiplier for Wireless Communication", Journal of Computers and Electrical Engineering, ISSN: 0045-7906, vol. 92, pp. 107178, June 2021. DOI: https://doi.org/10.1016/j.compeleceng.2021.107178.

19) Padma, P. Jagadamba, P. Ramana Reddy, "Implementation of High Performance FFT Architecture for DSP Applications", International Journal of Advanced Science and Technology, ISSN: 2005-4238, vol. 29, no. 3, pp.582-593, March 2020.

20) CH. Pallavi, C. Padma, R. Kiran Kumar, T. Suguna, & C. Nalini," Design of a 64-bit SQRT-CSLA with Reduced Area and High-Speed Applications in Low Power VLSI Circuits," Journal of VLSI Circuits and Systems, Vol.7, Issue.1, pp.40–45. March 2025.DOI: https://doi.org/10.31838/jvcs/07.01.06

21) C. Padma, S. B. Potladurty, C. Nalini, T. Suguna and C. Pallavi, "Efficient Approximate Adders for Image Processing Applications," 2024 International Conference on Advances in Computing Research on Science Engineering and Technology (ACROSET), Indore, India, 2024, pp. 1-6, Doi: 10.1109/ACROSET62108.2024.10743872.