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Performance Metrics Limitation And Solution For Designing CIC Decimation Filters For Wireless Communication

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Abstract: Cascaded Integrator Comb (CIC) decimation filters are widely employed in digital down-sampling systems due to their multiplier-less structure and hardware efficiency. However, their performance strongly depends on the filter order, which governs the trade-offs between spectral characteristics and implementation complexity. This study presents a comparative analysis of CIC decimation filters of different orders, evaluated in terms of passband ripple, stopband attenuation, power consumption, and hardware resource utilization. Simulation results indicate that higher-order CIC filters achieve improved stopband attenuation but at the cost of increased passband droop and higher power usage. Conversely, lower-order filters exhibit reduced hardware and power requirements but suffer from inferior spectral performance. The analysis highlights that optimal filter order selection is application-specific, requiring a balance between signal fidelity and implementation efficiency. The findings provide design guidelines for engineers to choose appropriate CIC filter configurations for low-power and resource-constrained wireless communication and signal processing systems with proper corrections.

Index Terms – CIC, decimation, wireless communication, low power

I. INTRODUCTION

In modern digital communication and signal processing systems, efficient sample rate conversion is essential for reducing data rates while preserving signal integrity. Among the various decimation filter architectures, Cascaded Integrator Comb (CIC) filters have gained significant attention due to their multiplier-less structure, scalability, and ease of hardware implementation. First introduced by Hogenauer, CIC filters eliminate the need for multipliers and rely solely on adders and subtractors, making them highly suitable for field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs).

The performance of CIC filters, however, is highly dependent on their order, which directly influences spectral and implementation characteristics. Increasing the filter order improves stopband attenuation, thereby enhancing the suppression of unwanted aliasing components. At the same time, higher orders introduce greater passband droop, leading to signal distortion in the desired band. Moreover, higher-order implementations demand more hardware resources and contribute to increased power consumption, which are critical design constraints in resource-limited and low-power applications.

Several studies have explored methods for compensating CIC filter drawbacks, such as passband droop correction and hybrid architectures. Yet, the fundamental trade-offs imposed by filter order remain a decisive factor in system design. A systematic comparison across different orders provides insights into the balance between signal quality and hardware efficiency, which is particularly valuable in the design of communication receivers, software-defined radios, and portable devices where both performance and power are critical.

This paper presents a comprehensive comparison of CIC decimation filters of varying orders, analyzed through four key performance metrics: passband ripple, stopband attenuation, power consumption, and hardware resource utilization. By highlighting the trade-offs among these parameters, the study aims to provide design guidelines for selecting an optimal CIC filter configuration tailored to application-specific requirements.

Key Performance Metrics of CIC Decimation Filters

Passband Ripple (ΔRp)

Passband ripple quantifies the variation in magnitude response within the passband. For CIC filters, the droop effect increases with order and decimation factor. It is defined as:

$$\Delta R_p = 20log_{10}\left(\frac{H_{max}(f)}{H_{min}(f)}\right), f \in [0, f_p] \qquad (1)$$

Where $H_{max}(f)$ and $H_{min}(f)$ are the maximum and minimum magnitudes of the frequency response within the passband f_p.

Stopband Attenuation (As)

Stopband attenuation measures the suppression of unwanted frequency components beyond the cutoff frequency. It is given by:

$$A_s = -20.log_{10}\left(\max_{f \in f_s}|H(f)|\right) \qquad (2)$$

Where f_s represents the stopband frequency range and $H(f)$ is the frequency response of the CIC filter. Higher order filters generally increase A_s.

Power Consumption (P)

Power consumption depends on the number of arithmetic operations (additions/subtractions) and the word length. A simplified expression for digital filter power is:

$$P \propto N_{ops}.V^2.f_{clk} \qquad (3)$$

Where N_{ops} is the number of arithmetic operations, V is the supply voltage, and f_{clk} is the clock frequency. For CIC filters, N_{ops} grows linearly with filter order.

Hardware Resource Utilization (HRU)

CIC filters use only adders, subtractors, and delay elements. Hardware resources are typically expressed in terms of registers (R), adders (A), and bit growth (B).

- Bit Growth due to accumulations is:

$$B = N.log_2(R.M) \qquad (4)$$

Where N is the filter order, R is the decimation factor, and M is the differential delay (commonly M=1).
Total hardware resources can be expressed as:

$$HRU = A + R + B \qquad (5)$$

Higher order filters require more registers and adders due to increased integration and comb stages

II. LITERATURE SURVEY

CIC filters, introduced by Hogenauer, have been widely analyzed due to their multiplier-less implementation and suitability for FPGA/ASIC integration. Recent reviews, such as [1], emphasize their efficiency in reducing memory and computational costs, while also outlining the inherent trade-offs between performance and hardware consumption.

The filter order plays a central role in shaping performance. As [2] discusses, increasing the order boosts stopband attenuation but simultaneously introduces greater passband droop, which must often be corrected through compensating filters. Similarly, [3] compared FPGA implementations and showed that higher-order CIC filters, while beneficial for alias suppression, consume more power and logic resources.

From a system-level perspective, oversampled sigma-delta ADC decimation filters highlight similar trade-offs. [4] demonstrated that order selection directly affects attenuation, ripple behavior, and circuit complexity, while [5] confirmed that CIC filters' reliance on adders and registers is advantageous for low-power design, but the bit growth problem scales rapidly with order and decimation factor.

Optimization approaches have been proposed. For example, [6] analyzed multiplier-free decimation filters and showed that design adjustments in filter order and architecture can balance area, power, and spectral performance. Similarly, [7] explored quantization-aware CIC designs, demonstrating reductions in gate count without significantly degrading frequency response.

Applications in software-defined radios and portable devices emphasize flexibility. [8] proposed channelization architectures where CIC filters serve as a first-stage decimator due to their efficiency, with compensating filters handling droop. For sensor systems, [9] designed low-power reconfigurable decimation filters where filter order could be tuned dynamically for power-performance trade-offs.

III. CASE STUDY CONSIDERING DIFFERENT ORDERS OF CIC DECIMATION FILTER

Key Findings from Literature

- Passband Ripple: Increases with filter order and decimation factor, requiring correction [2].
- Stopband Attenuation: Strongly improves with higher order, crucial for alias suppression [3]
- Power Consumption: Grows linearly with operations and word length; higher orders are costly for low-power devices [5].
- Hardware Utilization: More stages = more adders/registers and significant bit growth; quantization-aware optimizations help reduce resource usage [7].

Based on the key findings from the literature a case study is considered for CIC decimation filter of different orders. Here is a numerical comparison of frequency responses for 3rd, 4th and 5th order CIC filters with decimation factor R=8 and differential delay M=1:

Figure 1 shows the CIC filter frequency response when filter order is changed whereas the decimation factor (R=8) and differential delay (M = 1) are fixed. The sampling frequency is fs = 1 MHz It is clear that at least 4 stages of the CIC filter is necessary to provide sufficient attenuation.

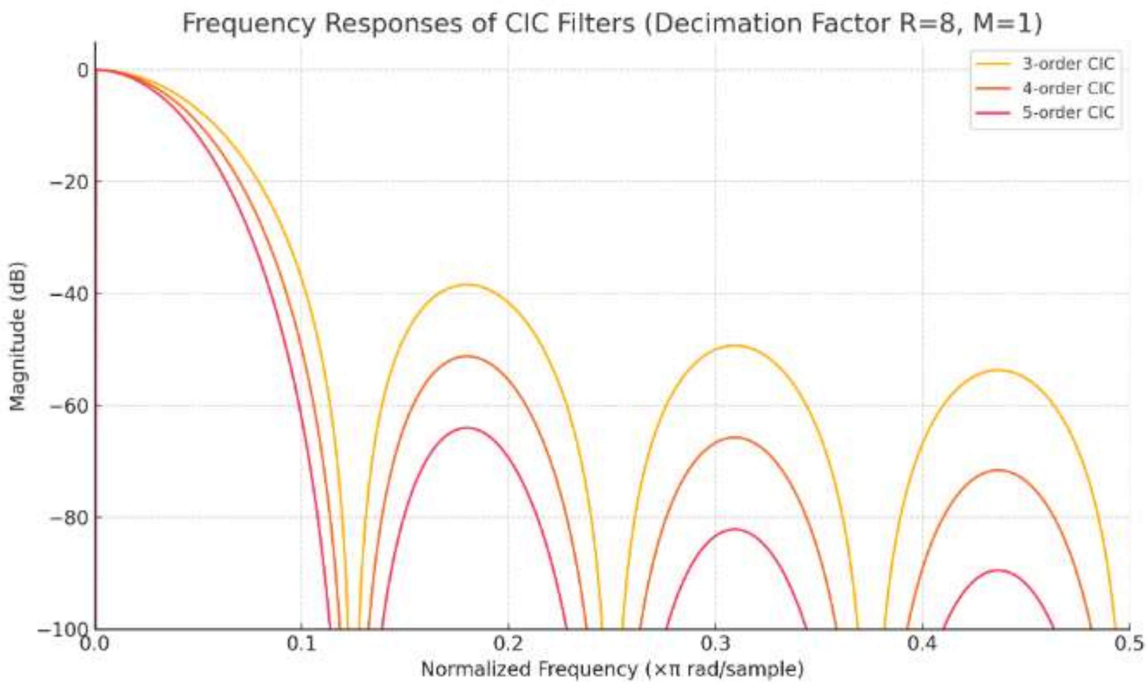

Figure 1: Frequency Responses of CIC Filters of Different Orders (Decimation=8, M=1)

From figure 1 it is observed that 3rd order CIC-filter has a Gentle roll-off, low passband droop and limited stopband attenuation.4th order CIC filter has Steeper attenuation and moderate passband droop, whereas for the 5th order CIC filter it is observed that it has strong suppression in the stopband, but severe passband droop and which needs corrections.

Based on equation 1 through 5 the calculation of performance metrics for all the three orders with decimation factor R=8 and differential delay M=1 is implemented and the same is shown in the table 1

Table1: Performance metric comparison for different order of CIC filters

S. No	Parameter	3rd Order CIC	4th Order CIC	5th Order CIC
1.	Passband Droop	0.561018	0.666372	0.746442
2.	Stopband Attenuation	7.16 dB	9.55dB	11.93dB
3.	Bit Growth	9	12	15
4.	Hardware Resources Integrator Adders Comb Subtractors Registers per stage	 3 3 8	 4 4 8	 5 5 8
5.	Estimated Dynamic Power	0.017mW	0.023mW	0.029mW

From the above analysis it is observed that to improve the performance of the CIC decimation filters corrections a re needed and the solutions to improve CIC Filter performance metrics are given in the table 2.

Table 2: Solutions to Improve CIC Filter Performance Metrics

S.No	Metric	Challenges	Solutions / Improvements
1	Passband Ripple [Mo, 2009; Hurrah et al., 2015; Lillington, 2003]	Higher order and large decimation factors increase passband droop.	Compensation filter: Append a low-order FIR/IIR filter to flatten the passband. Modified CIC (MCIC): Precompute correction coefficients to reduce droop. Sharpened CIC: Combine multiple CIC stages with weighted coefficients to improve flatness.
2	Stopband Attenuation [Madhav et al., 2023 Donnelly et al., 2017 de Freitas et al., 2025]	Limited by the inherent sinc^N response.	Sharpening technique: Use polynomial sharpening (e.g., Kaiser-Hamming) to increase sidelobe attenuation. Hybrid filtering: Add a lightweight FIR stage after CIC for sharper cutoff. Optimized differential delay ($M > 1$): Improves stopband suppression for certain designs.
3	Power Consumption [Cederström, 2009; Patil, 2016; Donnelly et al., 2017]	Increases with filter order, word-length, and high clock rates.	Pipelining and parallelism: Reduces critical path delay and dynamic power. Clock gating: Switch off inactive filter sections. Word-length optimization: Use minimum bit-width required to prevent overflow. Low-power FPGA mapping: Choose energy-efficient architectures (DSP slices vs LUT-based adders).
4	Hardware Resources [Adewale, 2023 Madhav et al., 2023 de Freitas et al., 2025]	Higher order filters require more adders, registers, and larger bit-width.	Resource sharing: Reuse arithmetic units across multiple stages. Optimized bit growth handling: Use saturation or truncation instead of full precision. Distributed arithmetic (DA): Efficient implementation for FPGA LUT-based designs. Hybrid CIC-FIR: Reduce CIC order and compensate spectrally with a small FIR, balancing hardware.

Considering the solutions stated in the table 2 following formulations are done. CIC filters are inherently efficient, but passband droop and limited stopband attenuation are their main drawbacks. The most common industry practice is a CIC + FIR compensation approach, where the CIC handles bulk decimation (cheap in hardware) and the FIR cleans up the spectral distortions.

1. CIC with Compensation Filter

The CIC filter performs efficient decimation, but introduces passband droop. A small FIR compensation filter is cascaded after the CIC to correct the passband response.

Overall Transfer Function:

$$H_{total}(z) = H_{CIC}(z).H_{comp}(z) \qquad (6)$$

Where:

$$H_{CIC}(z) = \left(\frac{1 - z^{-RM}}{1 - z^{-1}}\right)^N \qquad (7)$$

$$H_{comp}(z) \approx \frac{1}{H_{CIC}(e^{j\omega})} \qquad (8)$$

Thus, the compensation filter is designed to invert the passband drop of the CIC response.

- CIC Filter: Handles bulk decimation, efficient in hardware.
- FIR Compensation Filter: Low-order FIR, corrects passband flatness and sharpens stopband.

2. Sharpened CIC Filter

Sharpening uses polynomial combinations of CIC filters to enhance stopband attenuation and passband flatness without requiring an external FIR.

Sharpening Equation (Two-Point Kaiser-Hamming Method):

$$H_{sharpened}(z) = a.H_{CIC}(z)^2 + b.H_{CIC}(z) \qquad (9)$$

Where coefficients *a* and *b* are chosen to minimize passband droop and maximize stopband attenuation.

For example, a=1, b=-1 produces a first-order sharpening

Higher order sharpening yields better flatness b increases complexity.

- The outputs of CIC and its powered versions are linearly combined with weights a, b, …
- No external FIR stage is needed, but hardware grows with sharpening order.

Comparison of Techniques:

- CIC + FIR Compensation → Best balance, widely used in practice (low complexity FIR).
- Sharpened CIC → Attractive when FIR addition is undesirable (e.g., extreme low-power ASIC).

IV. Results and Discussion

Based on the above solutions the CIC decimation filters followed by FIR compensation filter are implemented for different orders and their performance metrics are calculated and tabulated as shown in the Table 3

Table 3: Performance metric comparison for different order of CIC decimation filter + FIR compensation filter

S.No	Parameter	3rd Order CIC	4th Order CIC	5th Order CIC
1.	FIR Taps	16	24	32
2.	Passband Droop	0.999143	0.999919	0.999992
3.	Stopband Attenuation	61.35 dB	81.79 dB	102.24 dB
4.	Bit Growth	9 bits	12 bits	15 bits
5.	Hardware Resources Integrator Adders Comb Subtractors Registers per stage	 3 3 8	 4 4 8	 5 5 8

Similarly, their frequency responses are also plotted for comparison in the figure 2(a) to 2(c)

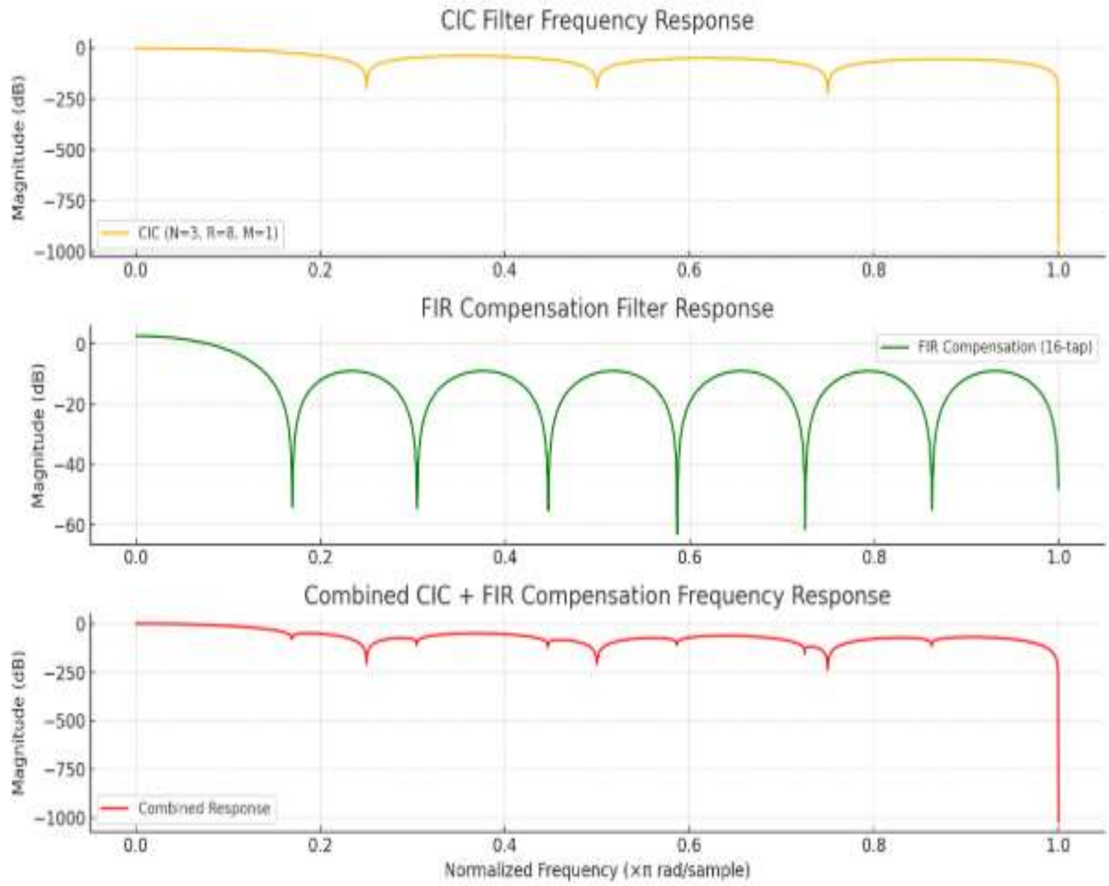

Figure 2 (a): Frequency Responses of 3rd order CIC Decimation Filter+ 16 tap FIR compensation filter (Decimation=8, M=1)

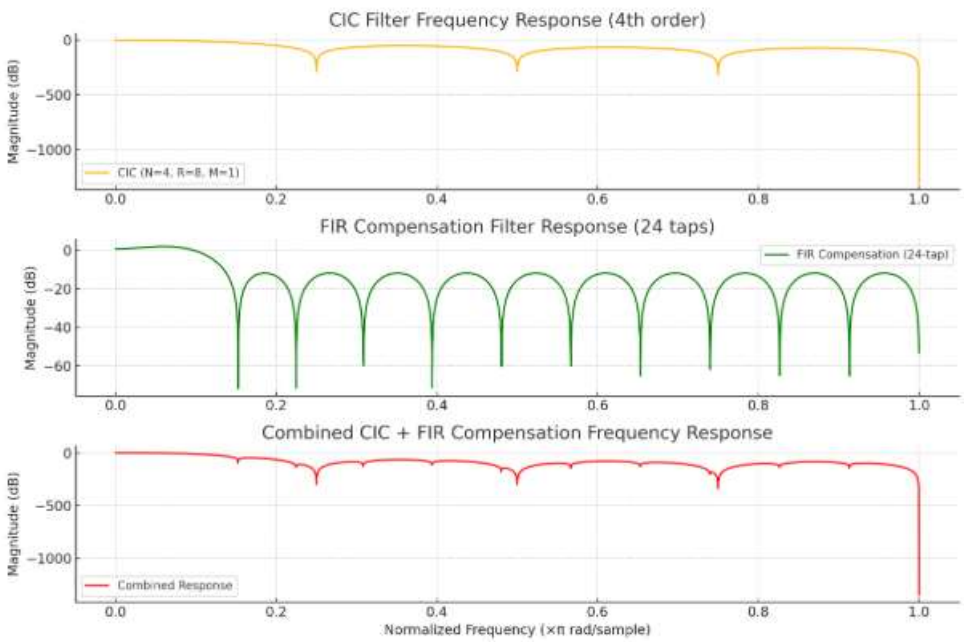

Figure 2 (b): Frequency Responses of 4th order CIC Decimation Filter+ 24 tap FIR compensation filter (Decimation=8, M=1)

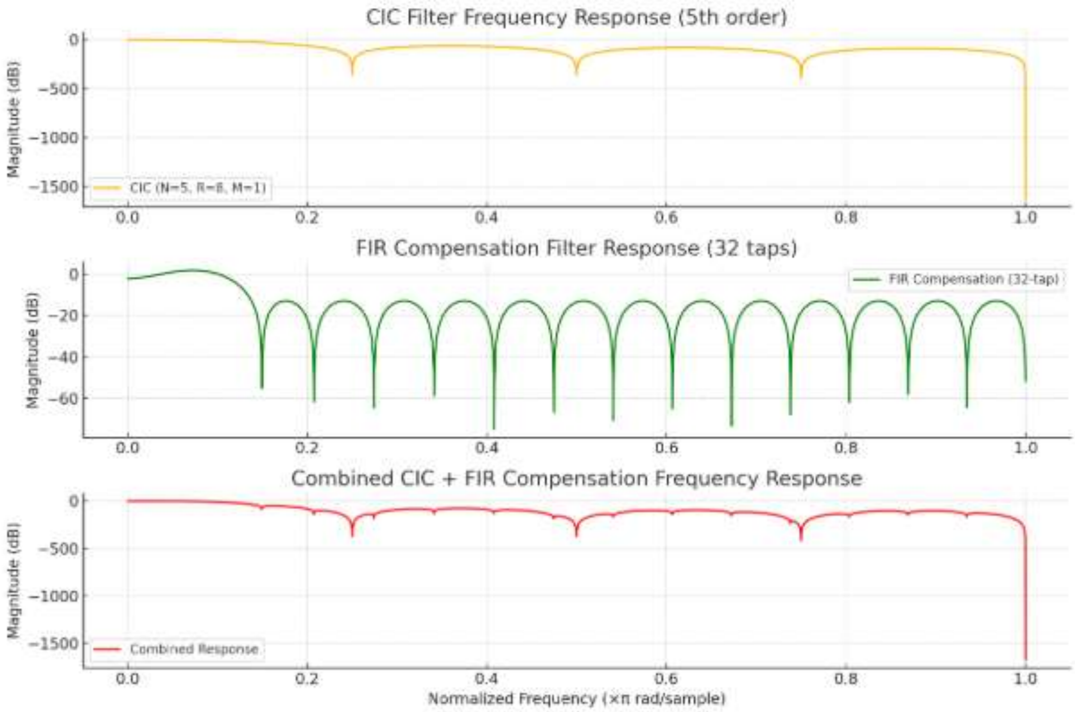

Figure 2 (c): Frequency Responses of 5th order CIC Decimation Filter+ 32 tap FIR compensation filter (Decimation=8, M=1)

The comparative evaluation of CIC decimation filters demonstrates the inherent trade-off between spectral performance and implementation efficiency as the filter order increases.

Raw CIC Filters: Higher-order CIC filters (4th and 5th order) provide improved stopband attenuation (from 7.16 dB in 3rd order to 11.93 dB in 5th order), but this comes at the expense of significantly larger passband droop, greater bit growth, and increased power consumption. For instance, the dynamic power rises from 0.017 mW (3rd order) to 0.029 mW (5th order).

CIC + FIR Compensation: Incorporating FIR compensation effectively corrects passband droop, raising the passband gain close to unity (0.9999), while substantially improving stopband attenuation (up to 102.24 dB for 5th order). However, this requires additional FIR taps (16, 24, and 32 respectively), increasing design complexity and hardware cost.

Overall, the findings suggest that:

- Low-order CIC filters are preferable for low-power and hardware-constrained applications, but need FIR compensation to meet spectral requirements.
- High-order CIC filters with FIR compensation provide superior spectral performance (flat passband and strong attenuation), but at the cost of higher complexity, bit growth, and power usage.

Thus, the choice of CIC filter order should be driven by application-specific constraints, striking a balance between signal fidelity and implementation efficiency.

V. Conclusion

The study confirms that higher-order CIC filters provide improved stopband attenuation but incur increased passband droop, bit growth, and power consumption. FIR compensation effectively restores passband flatness and enhances stopband suppression, though at the expense of added complexity. Therefore, the selection of CIC filter order remains application-dependent, requiring a balance between spectral performance and hardware efficiency. Future study can extend this work in different directions by using adaptive FIR compensation, hardware optimization, algorithmic trade-offs and application-specific evaluation.

REFERENCES

[1] A. Madhav et al., "A Brief Review on Hardware Efficient Cascaded Integrator Comb Filters," 2023 International Conference on Sustainable Communication Networks and Application (ICSCNA), Theni, India, 2023, pp. 858-863, doi: 10.1109/ICSCNA58489.2023.10370269.

[2] Daniel Mo "Power efficient ΔΣ bitstream encoder/decoder" 2009 Master thesis, UNIVERSITY OF OSLO Department of Informatics.

[3] Tim Donnelly et al., "A Comparative Study for Performance and Power Consumption of FPGA Digital Interpolation Filters" January 2017, International Journal of Advanced Computer Science and Applications 8(7) DOI:10.14569/IJACSA.2017.080766

[4] N. N. Hurrah, Z. Jan, A. Bhardwaj, S. A. Parah and A. K. Pandit, "Oversampled Sigma Delta ADC decimation filter: Design techniques, challenges, tradeoffs and optimization," 2015 2nd International Conference on Recent Advances in Engineering & Computational Sciences (RAECS), Chandigarh, India, 2015, pp. 1-6, doi: 10.1109/RAECS.2015.7453347.

[5] Love Cederström "Power Efficient Digital Decimation Filters for ΣΔ-ADCs" 2009 Master Thesis, Institution for systemteknik, Department of Electrical Engineering

[6] Otávio Elias Viana de Freitas et al., "Design and Optimization of Decimation Filters for Sigma-Delta ADCs" Journal of Integrated Circuits and Systems, Vol. 20 No. 1 (2025). DOI: https://doi.org/10.29292/jics.v20i1.961.

[7] Adewale, Ayomikun "The effect of coefficient quantization optimization on filtering performance and gate count" Master's Thesis, Faculty of information technology and electrical engineering, February 2023, University of Oulu

[8] J. Lillington "Flexible channelization architectures for software defined radio front ends using the tune able pipelined frequency transform" IEE Colloquium on DSP enabled Radio 2003 https://doi.org/10.1049/ic.2003.0326

[9] Satish Patil " Low Power Reconfigurable ΣΔ Modulator with Decimation Filter Design for Sensor Applications" Thesis for: MTech. Indian Institute of Technology Bombay. June 2016, DOI:10.13140/RG.2.1.5115.8007.