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DESIGN OF PLL USING SCL-180nm TECHNOLOGY

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Abstract: This work presents the design and analysis of phase-locked loops (PLLs) tailored for high-performance frequency and phase control applications. These PLLs are essential in systems requiring precise frequency synthesis, phase-aligned clock generation, and robust phase synchronization, particularly in wireless communication systems, RF front-ends, and high-speed data converters. The proposed PLL architecture is implemented using SCL-180nm CMOS technology, offering a practical trade-off between power efficiency and phase noise performance, while ensuring compatibility with modern integrated circuit fabrication processes.

Index Terms **- PLL, Phase-Locked Loop, Fractional-N, Integer-N, Frequency Synthesis, SCL-180nm, VLSI, Charge Pump.**

I. INTRODUCTION

Phase-Locked Loops (PLLs) are critical components in modern electronic and communication systems because they enable synchronization of a generated signal with a reference signal in both frequency and phase. Their importance stems from the following key functionalities:

- **Frequency Synthesis and Generation:**

  Multiple Frequency Generation: PLLs can generate a frequency range from just one reference frequency. This is critical in communication systems, which require multiple channels or bands.

  Fractional and Integer Frequency Multiplication: PLLs can work with precise frequency multiplication, allowing systems to generate fractional or integer multiple clocks from a reference frequency. These are applications in devices such as radio transmitters, receivers, and microprocessors.
- **Clock Recovery and Timing:**

  Data Synchronization: PLLs are embedded in clock recovery circuits for the recovery of timing information from any carrier signal. This is, once more, a very vital function of serial communication systems as accurate timing signals are needed at the time of data transmission.

  Clock Generation: PLLs in digital circuits are required to generate a clock signal that drives other components in a system in synchronization so that the integrity and stability of data are maintained.
- **Signal Stabilization:**

  Jitter and noise reduction: PLLs reduce phase noise and jitter in oscillators; hence, they increase the stability and quality of the generated signals. This is quite important for high-performance systems like RF communications, where clarity of signal is paramount.

  Stabilizing with a stable reference: PLLs are used to lock the frequency of a system to a stable reference oscillator.

  This is quite critical in maintaining the consistency and reliability of communication signals.

- **Modulation and demodulation:**
  FM Demodulation: PLLs are used in FM receivers to demodulate the incoming signal by tracking its frequency changes.
  Phase Modulation: PLLs are also used in phase modulation schemes, used with great frequency in the digital communication systems such as Phase-Shift Keying (PSK).
- **Applications in Communication Systems:**
  RF Transceivers: PLLs perform the task of translating the baseband signal to RF and vice versa in radio frequency communication systems, thereby enabling the successful transmission and reception of signals.
  Synthesizers in Wireless Devices: PLL forms the heart of the frequency synthesizers in all wireless devices that let it tune to different frequencies and channels on cellular networks, Wi-Fi, Bluetooth, and other such technologies.
- **High-Speed Data Converters:**
  Timing ADCs/DACs: PLLs provide timing ADCs and DACs with accurate clock signals, which make the sampling and conversion rates very accurate.
- **Control Systems:**
  Feedback Control: PLLs find application in control systems meant to maintain various elements of the system in phase by adjusting the phase and frequency of control signals to obtain consistent performance.

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. The PLL architecture is envisioned to lock the phase of a generated signal to the phase of a reference signal. The concept is key to a number of electronic applications, such as frequency synthesis, clock generation, and signal modulation.

A. Basic Components of a PLL

The simplest PLL constituents can be summarized as follows:

- Phase Detector or Phase Frequency Detector.
- Low Pass Filter.
- Voltage-Controlled Oscillator.
- Frequency Divider.

B. Phase Detector PD/Phase Frequency Detector PFD

Function: It compares the phase of an input reference signal with that of the signal from the VCO, after division if a divider is used. It will produce a phase error signal proportional to the phase difference between the two signals. Some designs include a Phase Frequency Detector (PFD) that detects the phase difference and the frequency differences, thus making a PLL more robust and able to lock when the input and VCO frequencies are different.

Types:

i. Analog Phase Detector: Generally used for analog PLLs. It multiplies the two input signals to provide an output proportional to the phase difference.
ii. Digital Phase Frequency Detector (PFD): This is used in digital PLLs. It produces a pulse width that is directly proportional to the phase difference and proves better in those applications where large capture ranges are needed.

C. Low Pass Filter (LPF)

Function: The Low Pass Filter (LPF) cleans the phase detector output by removing high-frequency components, so only a smooth DC control voltage remains. This control voltage is applied to the VCO to modulate its frequency for locking the phase with the input signal. It will also characterize the dynamic behavior of the PLL, such as lock time and loop stability.

There are 2 types of LPF.

A passive low pass filter is typically composed of simple RC (resistor-capacitor) networks. These filters are easy to design and implement, making them a popular choice for basic applications. However, they often fall short when it comes to providing optimal stability and noise rejection. Their performance is limited due to the absence of active components, which restricts their ability to fine-tune the loop characteristics. As a result, passive filters may not be suitable for high-performance or precision PLL applications.

An active low pass filter incorporates operational amplifiers along with passive components. These filters offer much more precise control over loop dynamics and provide superior filtering capabilities compared to passive filters. Active filters can significantly enhance the stability and

noise performance of the PLL system. They are particularly useful when fine control of loop bandwidth and phase margin is necessary, making them ideal for advanced communication and high-speed digital systems.

D. Voltage-Controlled Oscillator (VCO)

A Voltage-Controlled Oscillator (VCO) is a critical component of a Phase-Locked Loop (PLL) system. It generates an output signal whose frequency is directly proportional to the applied input control voltage. The VCO adjusts its frequency dynamically based on the control voltage derived from the feedback loop. This feedback mechanism allows the VCO to lock onto the desired output frequency defined by the reference signal. The ability of the VCO to vary its frequency precisely makes it indispensable for frequency synthesis, modulation, and timing recovery in communication and digital systems.

Types of VCOs:

A linear VCO exhibits a linear relationship between its output frequency and the control voltage. These are predominantly used in analog PLLs where smooth and continuous frequency variation is required. Their linear behaviour simplifies loop filter design and analysis.

Digital VCOs are commonly used in digital PLLs and are typically implemented using ring oscillators or LC oscillators. These designs are more compatible with digital circuitry and offer better integration in modern digital systems. While they may not always offer perfect linearity, their ease of implementation and compatibility with CMOS technology make them popular in low-power and high-speed applications.

E. Frequency Divider

A **frequency divider** is an integral component of many PLL architectures. Its primary function is to divide the output frequency of the Voltage-Controlled Oscillator (VCO) before it is fed back to the phase detector. By doing so, the PLL can lock onto a multiple of the reference frequency and produce higher or variable output frequencies. Frequency dividers can be implemented as either fixed or programmable circuits. They are especially important in **frequency synthesis** applications where multiple output frequencies are required from a single reference source.

Types of Frequency Dividers:

- Integer-N Divider: The Integer-N frequency divider divides the VCO output frequency by a fixed integer value (N). This method is simple and efficient, making it suitable for many straightforward frequency generation tasks. However, its limitation lies in its coarse frequency resolution, as the output frequency can only be changed in large steps defined by integer multiples of the reference frequency.
- Fractional-N Divider: The Fractional-N divider enhances the functionality of the PLL by enabling division of the VCO frequency by a fractional (non-integer) value. This allows for finer control over the output frequency, supporting more flexible and precise frequency synthesis. This capability is crucial in communication systems where high frequency resolution and agility are needed.

Incorporating a frequency divider within a PLL offers several important benefits. Most notably, it allows the PLL to operate over a broader frequency range by scaling down the VCO frequency. This enables the generation of both lower and higher frequencies from a single reference clock, enhancing the flexibility of the system.

Additionally, by allowing the VCO to operate at higher frequencies—where it typically exhibits better performance characteristics—while still producing lower, manageable output frequencies, the divider contributes to overall PLL efficiency and signal quality. This division improves the accuracy and stability of the output frequency, which is essential for applications in clock generation, modulation, and wireless communication systems. In frequency synthesizers, the use of dividers is particularly advantageous for generating multiple, stable frequency channels from a single input source.

II. Literature Review

Significant progress has been made in the design and performance of various Phase-Locked Loop (PLL) architectures, particularly in the realm of digital PLLs and frequency synthesis. This section presents a review of notable contributions from recent literature, highlighting key innovations and performance enhancements across multiple PLL designs.

Pradhan and Jana (2021) [1] introduced a CMOS-based precharged phase frequency detector (PPFD) specifically for phase-locked loops. Their design focused on optimizing performance metrics such as output behavior and power consumption. Operating across a frequency range of 1.25 MHz to 3.8 GHz, the circuit minimizes reset time to enhance overall performance. Importantly, the PPFD demonstrates low power consumption and improved phase noise characteristics, making it well-suited for low-noise PLL applications.

Tsai et al. (2020) [2] proposed a hybrid PLL architecture that combines an all-digital PLL with a charge-pump PLL. Through phase realignment, the design achieves a settling time of just 0.6 μs and an integrated jitter of 0.619 ps. Fabricated in 7-nm FinFET technology, the implementation reaches a state-of-the-art figure of merit (FoM) of -240.5 dB. This hybrid architecture exemplifies modern advances in high-speed, high-performance PLL design with significant implications for integrated systems.

In a 2023 study, Zhong et al. [3] reported a fully ring-oscillator-based cascaded fractional-N PLL operating up to 4 GHz. The design features a compact active area of just 0.016 mm^2 and incorporates burst-mode sampling for enhanced performance. The architecture demonstrates how power efficiency and high-frequency performance can be achieved simultaneously, showcasing promising developments in compact, low-power PLL solutions.

Yang et al. (2022) [4] proposed a harmonic mixing PLL architecture aimed at millimeter-wave applications. This architecture addresses several intrinsic limitations of traditional PLLs operating at high frequencies. By employing new mixing mechanisms, the harmonic mixing approach enables improved integration and performance, expanding the application of PLLs into the millimeter-wave spectrum.

Magerramov and Zaitsev (2021) [5] investigated the impact of low-pass filter design, comparing active and passive filtering methods on PLL performance. Their work, presented at the IEEE Conference of Russian Young Researchers, provides detailed insights into how filter selection influences key performance trade-offs, such as noise, stability, and response time. This comparative analysis is valuable for designers seeking to balance complexity and efficiency in PLL systems.

Wan et al. [6] introduced a bias-current-free PLL fabricated in 14 nm FinFET CMOS technology, which supports a frequency range from 0.54 GHz to 1.76 GHz. By eliminating the need for bias currents, the design simplifies circuit implementation and reduces power consumption. With a compact area of 0.0048 mm^2 and a wide voltage range from 0.43 V to 1.0 V, the architecture is highly adaptable to various modern low-power applications.

Lastly, a technical report from Texas Instruments [7] serves as a practical reference for PLL and frequency synthesis. It offers detailed guidance and real-world examples, contributing significantly to the understanding of design considerations, implementation techniques, and performance optimization in PLL systems.

III. Problem Statement

Design and analysis of a Phase-Locked Loop (PLL) pose a number of fundamental challenges that need to be met to guarantee stable, robust, and high-performance operation over an extended frequency range. The design requires a delicate optimization of performance, power, stability, and integration.

One of the most important issues is the management of frequency range. The PLL needs to be able to lock and keep phase coherence across the entire operational frequency band reliably. This means choosing or designing components—like Voltage-Controlled Oscillators (VCOs) and frequency dividers—that perform well and consistently over broad frequency ranges.

Another serious problem is phase noise and jitter reduction. Having a clean and stable output signal is crucial in both analog and digital systems. Phase noise and jitter in excess of acceptable levels can compromise signal integrity and lead to timing errors, especially in high-speed communication and data conversion systems.

Bandwidth and loop stability are another key design problem. The designer has to balance the loop bandwidth to satisfy the speed and response time specifications and ensure overall system stability. A too-wide bandwidth can create spurious tones and instability, and an insufficiently wide bandwidth can restrict the PLL from properly tracking frequency and phase changes.

Power consumption must also be carefully controlled, especially across different operating frequencies. As frequency increases, so does the demand for power, and the PLL must be designed to deliver high performance without incurring excessive power usage. Efficient power management becomes essential in battery-powered or thermally sensitive applications.

In addition, the operation of individual building blocks, like the VCO, Phase Frequency Detector (PFD), and charge pump, is also critical. These must be not just high-performance but also robust and stable across the whole frequency range. Non-linearity or mismatch in any of them can notably degrade overall PLL performance.

Physical layout and integration are challenging, especially at high frequencies where parasitic inductance and capacitance can impact performance. The PLL has to be small and highly integrated with minimal layout-induced degradation to be manufacturable and scalable in today's systems-on-chip (SoCs).

Finally, test and validation are needed to ensure that the PLL functions as designed throughout its entire frequency range. Detailed test procedures need to be designed to test lock time, phase noise, jitter, and frequency accuracy in all operating conditions and to meet the designed specifications.

IV. OBJECTIVES

The architecture of the Phase-Locked Loop (PLL) will be designed and implemented with the Cadence tool suite, which provides end-to-end capabilities in schematic design, simulation, layout, and verification. The design flow involves some of the most important building blocks of the PLL: Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage-Controlled Oscillator (VCO), and Frequency Divider.

The Phase Frequency Detector (PFD) compares the reference signal's phase and frequency with the divided VCO output's feedback signal. The PFD produces an error signal that controls the charge pump. The PFD's architecture selected should have minimal dead zone to make the detection of phase precise and continuous, which is essential for quick acquisition and precise locking in the PLL.

Subsequent to this, the Charge Pump is coupled with the PFD. Its purpose is to convert the PFD's logic-level error signals into an analog control voltage that controls the frequency of the VCO. The charge pump must be designed carefully to ensure loop stability; it must have low output noise and low charge sharing, which are critical in avoiding spurious tones and phase jitter.

The Loop Filter has a crucial function in determining the dynamics of the PLL. It filters the pulsed input of the charge pump to generate a stable control voltage for the VCO. The loop filter design needs to be optimized depending on the target loop bandwidth to achieve the best trade-off between settling time and phase noise performance. The filter also determines the phase margin and system stability.

The Voltage-Controlled Oscillator (VCO) is the frequency-generation component of the PLL. The frequency of the VCO is controlled by the loop filter's control voltage. Particular care will be taken to keep phase noise as low as possible since it is directly responsible for the quality of the output signal as well as the PLL's performance. The architecture of the VCO and its tuning behavior have to accommodate the wide range of operation and the linearity requirements of the design.

Finally, a Frequency Divider is utilized in the feedback loop of the PLL. The divider allows the PLL to lock onto a multiple of the reference frequency and is the key component of frequency synthesis. Two divider types will be discussed: the Integer-N Divider that has coarse frequency stepping, and the Fractional-N Divider that has fine resolution of output frequency. The step size is controlled by the division ratio to provide high-precision frequency tuning in different applications.

V. IMPLEMENTATION

Phase Frequency Detector (PFD)

Phase characteristics and its effects: A Phase-Locked Loop (PLL) is a form of a feedback system where the phase of the input signal is aligned with that of the reference signal. There are various PLL architectures. However, we will opt for a Charge-Pump PLL. Type I PLLs are much more straightforward, but they have considerable trade-offs between the loop bandwidth (ω_{LPF}) and the damping ratio (ζ), and have a limited acquisition range. To overcome the acquisition problem, the design uses frequency and phase detection. For periodic signals in systems, one can combine the frequency and phase feedback loops-the function of which is taken over by Phase Frequency Detector (PFD).

Figure.1 Elaborates clearly how the operation of the Phase Frequency Detector works. Assume that Q_a and Q_b are set to zero. Input A transitions high before input B does and so Q_a goes HIGH, Q_b remains low. The state persists until input B does go high; at this point Q_a will then reset back to zero, with Q_b still at zero. A similar mechanism takes place for Q_b and Q_a when input B increases before input A. From Figure.1(a) it is quite evident that Q_a points to the phase difference ($\Phi A - \Phi B$) between the inputs, whereas in Figure.1(b), Q_a points to the frequency difference ($\omega A - \omega B$) between the inputs.

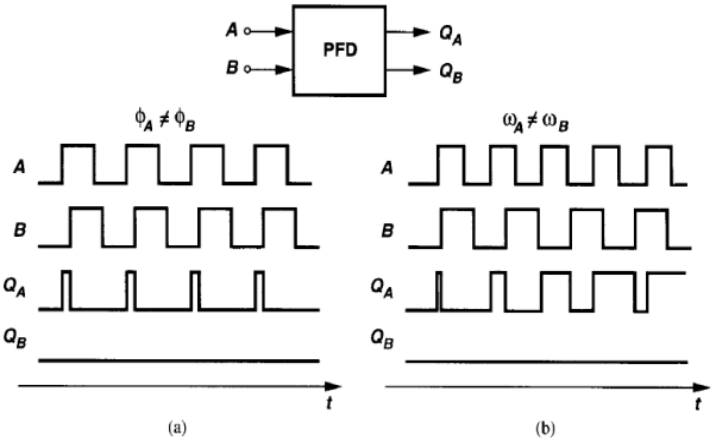

Figure 1: PFD Operation

The phase error $\Delta\phi$ due to phase characteristics is given by:

$$\Delta\phi = \Delta t / T \cdot 2\pi$$

where T is the total time period.

The gain of the Phase Frequency Detector (PFD), KPFD, is expressed as:

$$KPFD = Vdd / 4\pi$$

where Vdd is the supply voltage, and 4π represents the total linear range.

Alternatively, the gain can be defined in terms of the charge pump current Icp as:

$$KPFD = Icp / 2\pi$$

Standard PFD Architecture

Traditional NAND-based PFD normally makes use of a state machine with memory elements and, thus involves six two-input NAND gates and three three-input NAND gates. Since the gates used are NAND in nature, this can make the system bulky and may result in non-ideal effects. The ideal PFD should show linear output characteristics for all phase differences from 0 to 2π.

However, deviations from this ideality can cause faulty output of information that will then decrease the phase comparison range, which eventually limits the operation frequency of the PFD. This limitation increases the time taken for frequency acquisition in a phase-locked loop (PLL).

In the basic functioning of a PFD, the outputs, namely, UP and DN, are low 2. When the reference frequency, F_{ref}, is high, the UP output becomes high. This state prevails until the frequency of feedback is also taken high to reset the output. It then comes back to the low state from where it started. With the increase in operating frequency required by the PFD, other parameters such as phase noise and power consumption accelerate and hence degrade in their performance, which leads to the degradation in the performance of the PFD.

Advanced approaches for these design challenges include PFDs, pass transistor logic, and latch-based PFDs. Other new designs include fast frequency acquisition PFDs, which ensure a reduced dead zone and blind zone in the new designs. Still, most of the new designs are digital PFDs; then, digital PFDs can be more power- and area-intensive. This work mainly focuses on reducing the dead zone and blind zone of the PFD while increasing the input range. As a result of this approach, the possibilities of cycle skipping due to large phase differences between the inputs F_{ref} and F_{div} are reduced; hence, the speed of lock acquisition of the PLL will be increased.

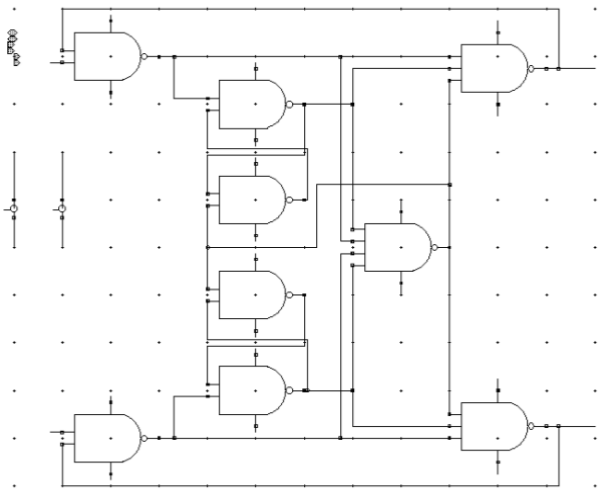

Figure 2: Standard PFD Schematic

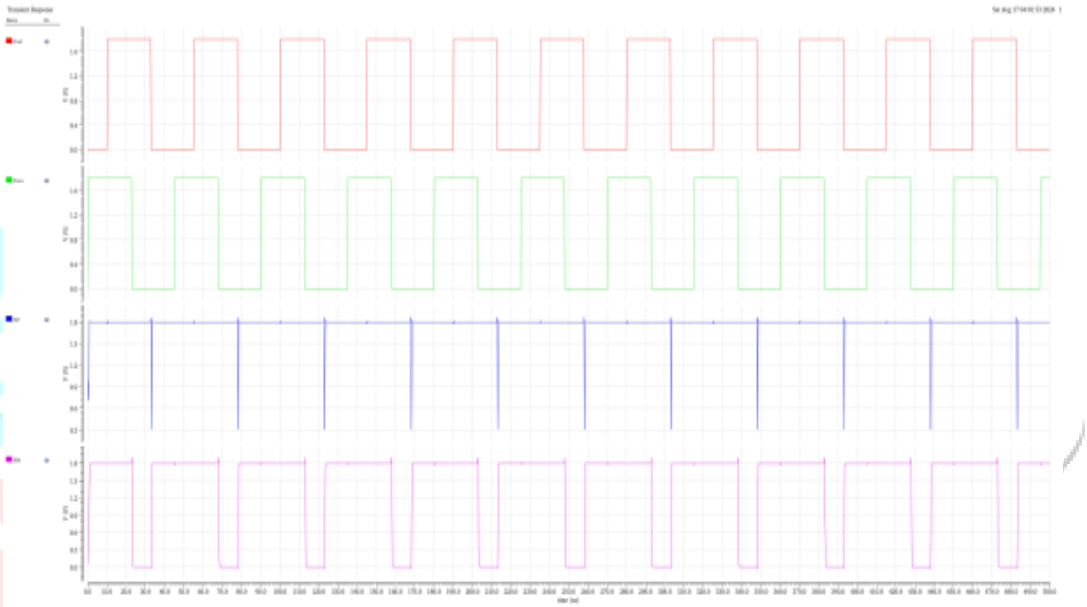

Figure 3: Standard PFD Output Waveform with reference frequency lagging

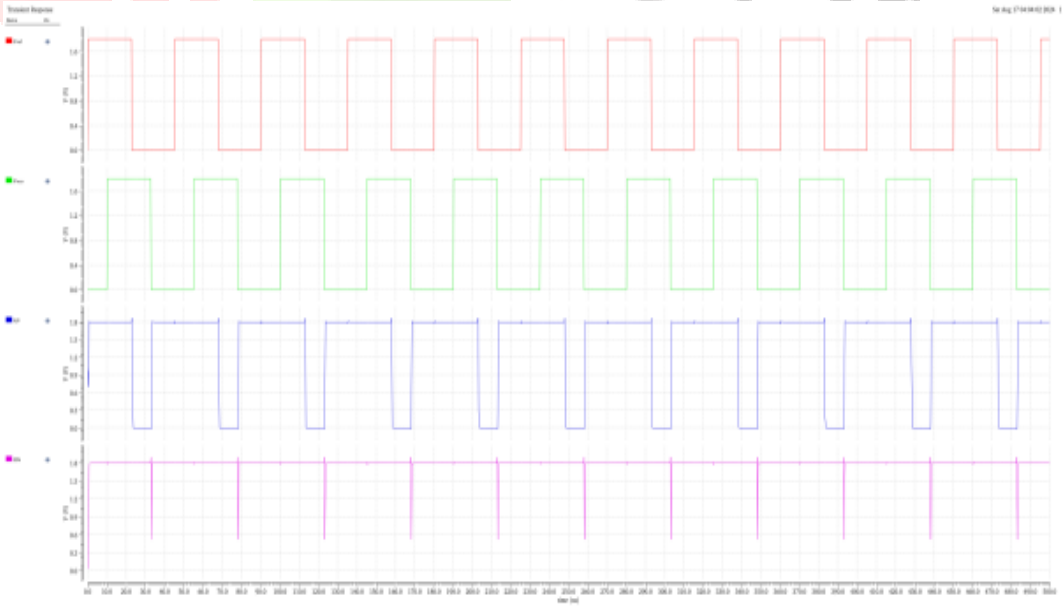

Figure 4: Standard PFD Output Waveform with frequency from vco is lagging

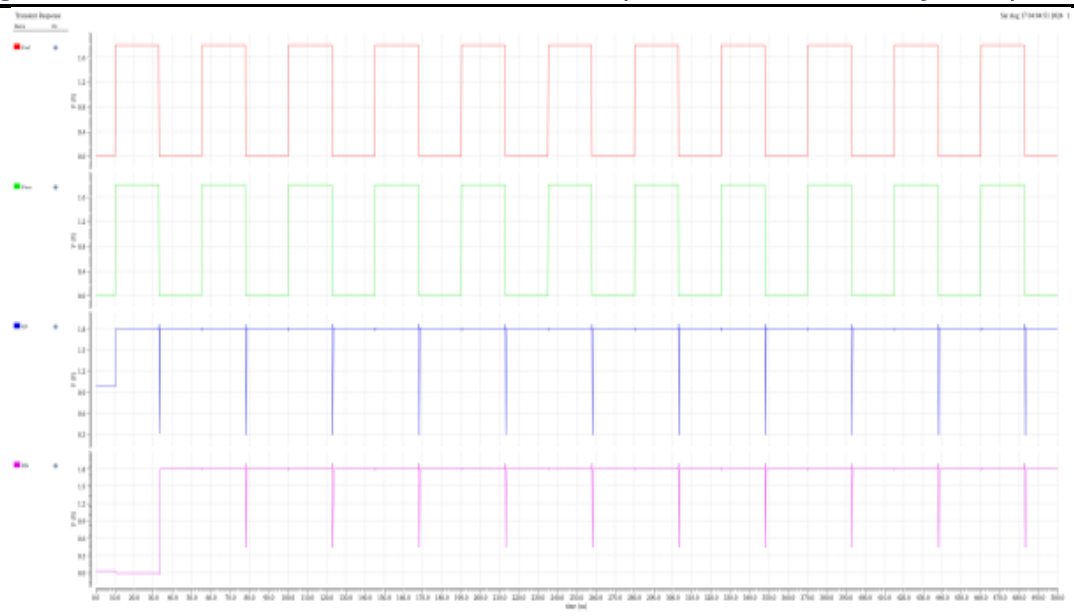

Figure 5: Standard PFD Output Waveform with Fref=Fvco

Precharge PFD

This design contributes a small Tchp to the blind zone, expressed by Tres+TD+Tchp. It has been found that Tres is a critical factor in reducing the blind zone. On the other hand, to avoid the dead zone, a delay is added to the reset path of the PFD, which generates a narrow pulse. However, this additional delay in the reset path limits the phase comparison range to less than 2π. To address this, we will use a PFD design that reduces both blind and dead zones, thereby improving phase noise performance, as shown in Figure 6.

The PFD offers the advantage of immediate reset upon detecting an undetermined state at the output. This is achieved by incorporating a newly added pull-down path, which re-quires four additional transistors: M10, M11, M21, and M22. Consider the following cases to understand the functionality of the proposed PFD:

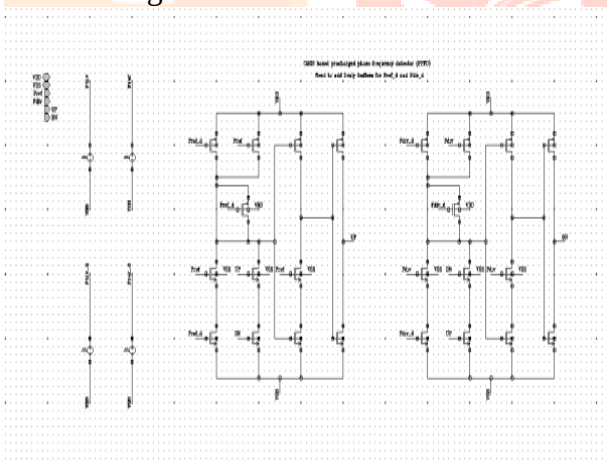

Figure 6: Precharge PFD

- Case I (Initial State): When both inputs, F_{ref} and F_{div}, are at logic ’0’, the output of the first stage (node T1) is also ’0’. This causes M5 to charge up, resulting in the output of the second stage becoming ’1’, while the final output remains ’0’.
- Case II (When F_{ref} Leads and F_{div} Lags): When F_{ref} goes high, the ’UP’ signal becomes active until the F_{div} signal turns on the ’DN’ signal, which returns the output to its previous state. When both ’UP’ and ’DN’ signals are high, the pull-down transistors M10, M11, M21, and M22 are activated. This pulls the logic ’1’ output at nodes T1 and T2 down to ’0’, thus resetting the output to its previous state. The pulse width of the output depends on the discharge time through these transistors. Eliminating the traditional reset reduces the reset time, which improves the maximum operating frequency, expressed by:

$$f_{ckref} \approx 1 / 2.\ t_{res}$$

where f_{ckref} is the clock reference frequency.

This equation indicates that a decrease in reset time t_{res} leads to an improvement in the maximum operating frequency. Additionally, using a higher reference frequency (F_{ref}) Figure 8. TSPC PFD increases the loop bandwidth, thereby enhancing the PLL’s locking time.

- Additional Consideration: Furthermore, when the phase difference between the two inputs approaches 2π, the rising edge of the leading signal may coincide with the reset operation, potentially causing a skipped cycle. To ensure that this skipped cycle appears at the output, the design includes two transistors, MX and MY, as shown in Fig6. These transistors pull nodes T1 and T2 to logic high using inputs F_{refd} and F_{divd}, respectively.

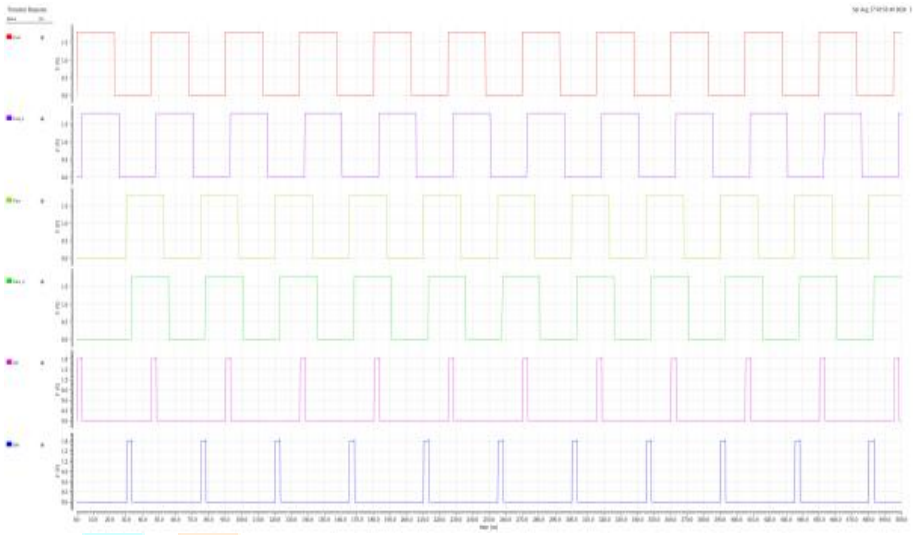

Figure 7: PPFD Output Waveform

True Single Phase Clocked (TSPC) PFD

TSPC is a single-phase clock-based design technique that allows fast operation. It reduces power consumption and complexity compared with conventional dual-phase clocked designs. The PFD design is show below in Figure 8.

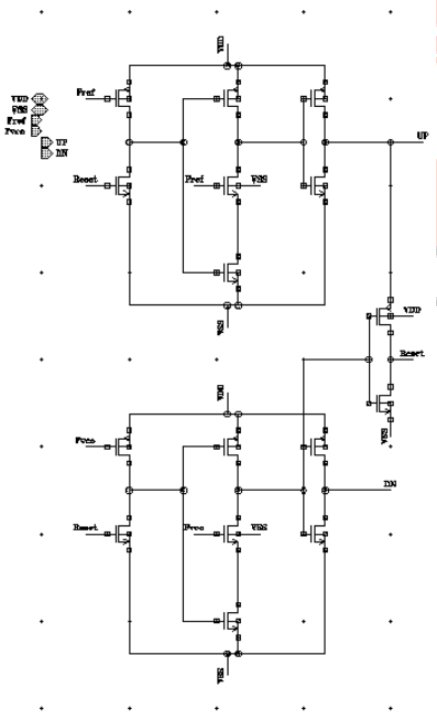

Figure 8: TSPC PFD

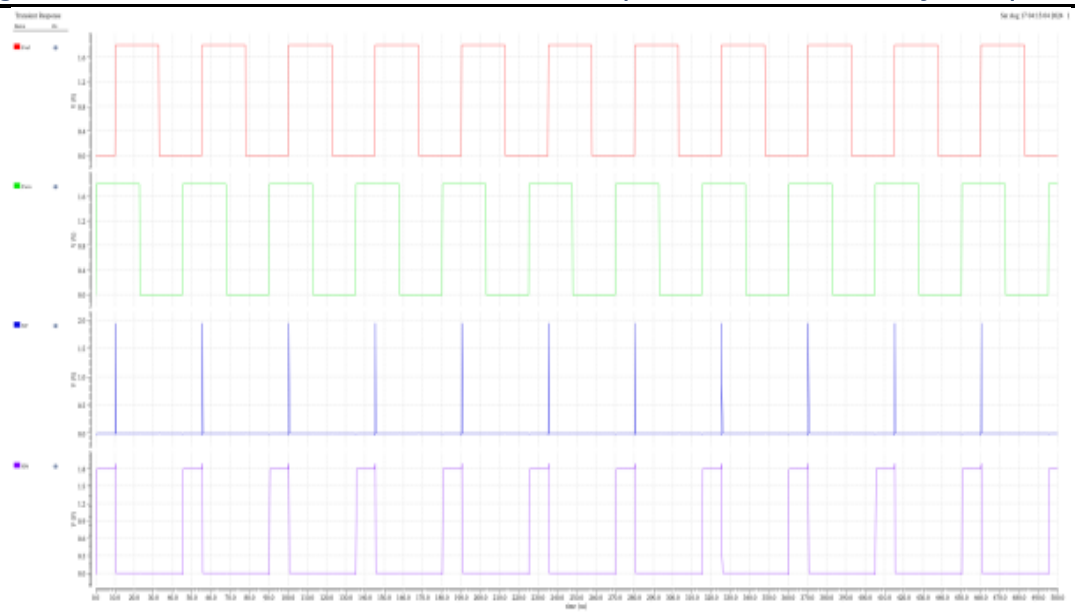

Figure 9: TSPC PFD Output Waveform with reference frequency lagging

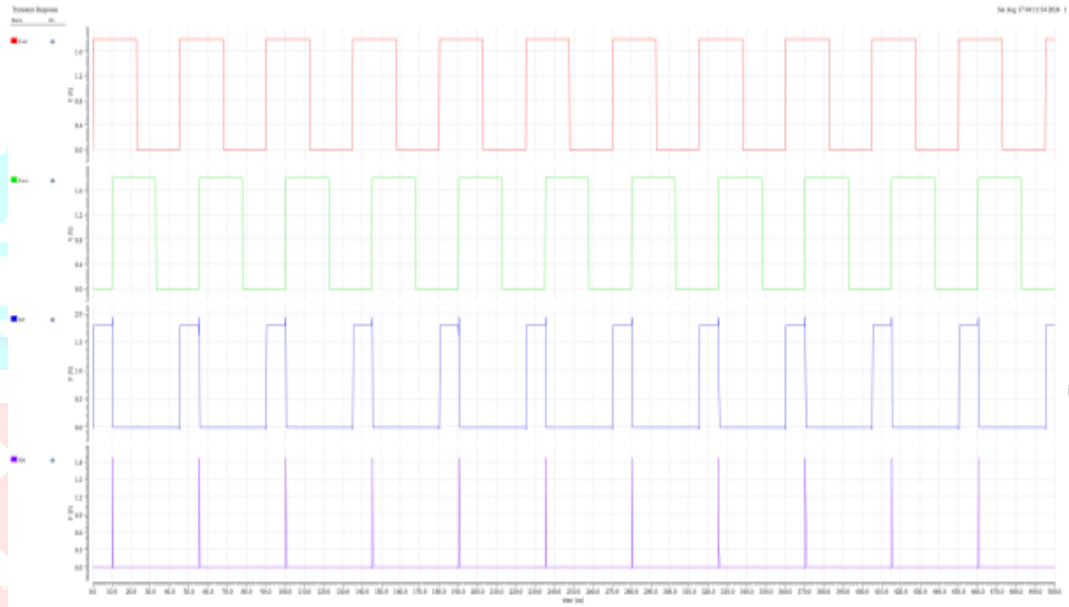

Figure 10: TSPC PFD Output Waveform with frequency from vco is lagging

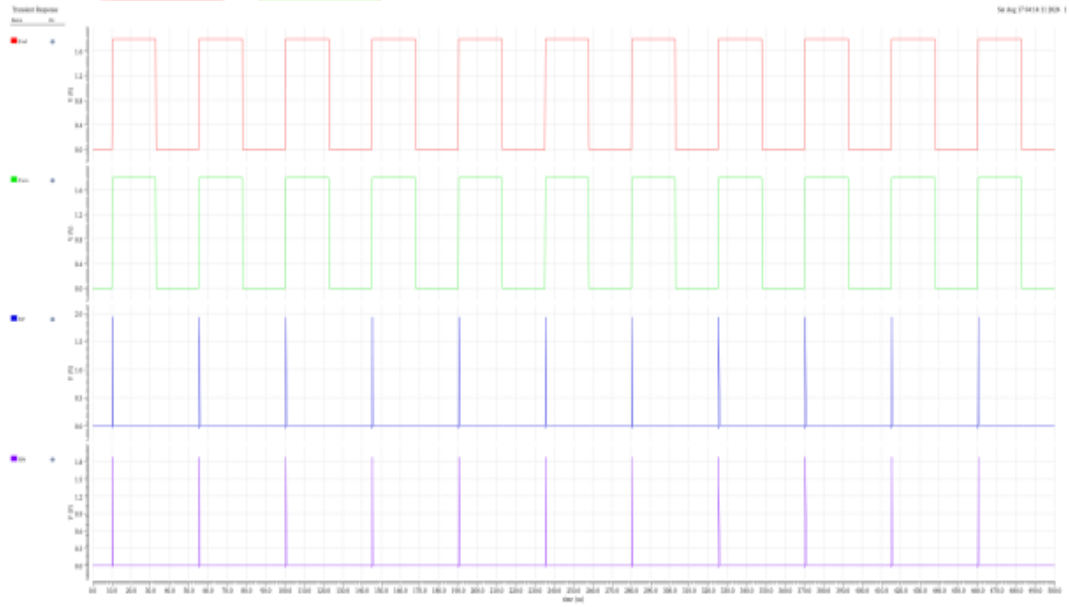

Figure 11: TSPC PFD Output Waveform with Fref=Fvco

Charge Pump (CP)

A charge pump is essentially two switched current sources, which push charge into or pull charge out of the loop filter based on the logic states of Q_a and Q_b. The two currents, I1 and I2, are typically the same magnitude and are called the Up and Down currents, respectively.

A charge pump can be realized using MOSFETs, as is schematically illustrated in Figure Figure 12(a). Here M1 and M2 are current sources, whereas switches are M3 and M4. But there appears a glaring drawback because of different arrival times of input signals at the charge pump, owing to an inverter being introduced. This delay can be compensated for by inserting a transmission gate between Q_b and the gate of M3, which tends to match the delays, as in 12(c).

The design thus far can be modified to eliminate bootstrap-ping, which is a problem that arises from the finite capacitance measured at the drains of the current sources. For example, as illustrated in Figure 13, when switches S1 and S2 are not asserted, the capacitor CX discharges to ground, and CY charges to VDD. When both S1 and S2 are asserted, the voltages VX and VY are roughly equal to V_{cont} provided a minimal voltage drop across S1 and S2. Even though the phase error is zero and ID1 equals ID2, and CX equals CY, then VX and VY do not change equally, creating a sudden jump in V_{cont}, which should ideally remain stable. The difficulty of this reveals a problem that will not be solved here.

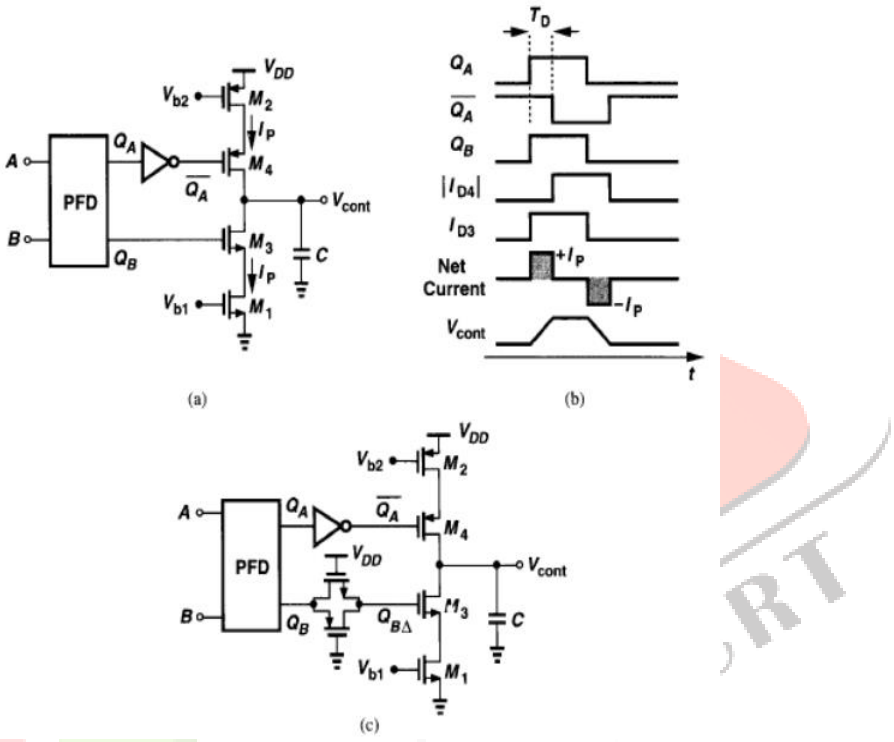

Figure 12: (a) Implementation of Charge Pump, (b) Effect of skew between Q_a and Q_b, (c) Suppression of skew by transmission gate

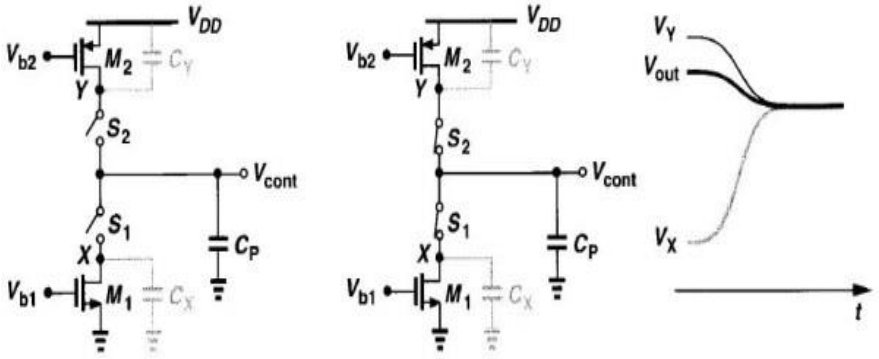

Figure 13: Bootstrapping

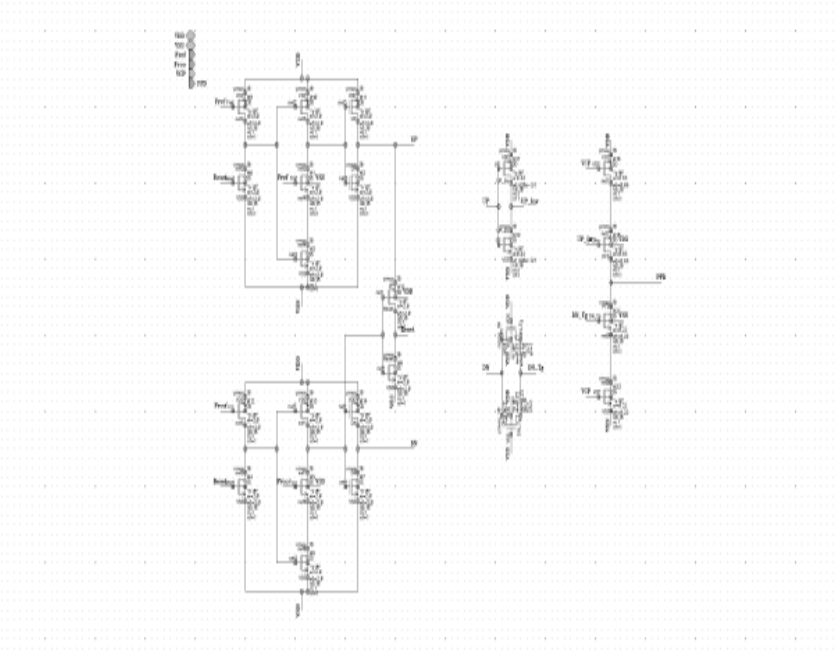

Figure 14: Designed TSPC PFD with CP

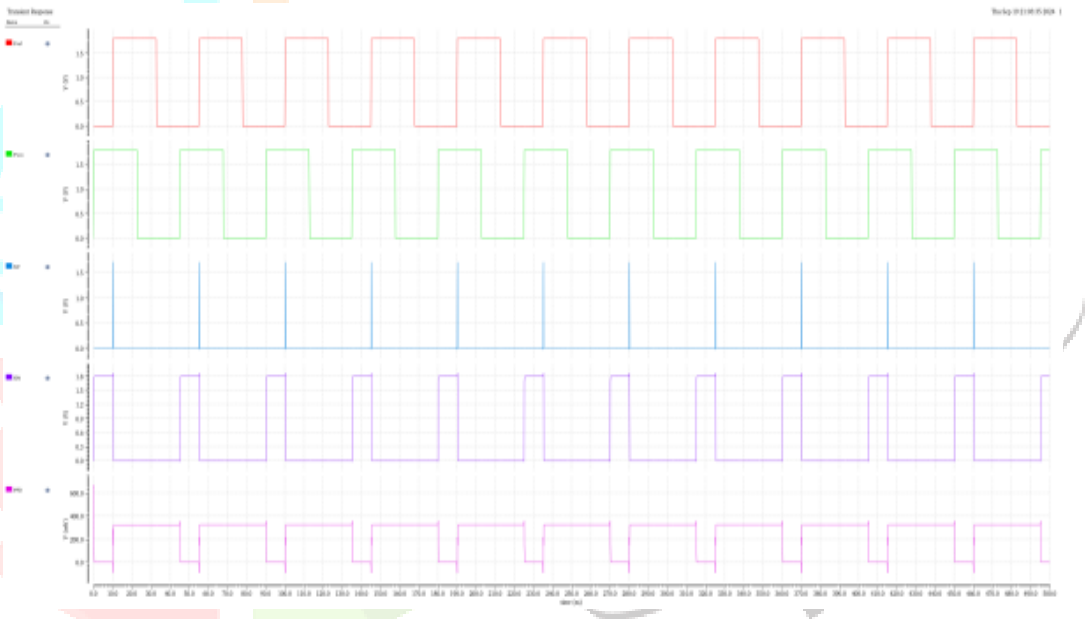

Figure 15: PFD with Charge Pump Output Waveform

Low Pass Filter

The LPF is the filter which has a characteristic of allowing only low frequency components to pass and blocking un-wanted higher frequencies. The selection of a filter circuit to-tally depends upon the specific design requirements of Phase-Locked Loop (PLL) such as the desired cutoff frequency, the level of noise and jitters present in the phase detector output, and the response time of the PLL.

The cutoff frequency fc is given by the formula:

$$f_c = 1/2\pi T$$

where f_c is the cutoff frequency and T is the time constant of the Low pass filter.

The main types of low pass filter are numerous, but the most common is RC. An RC low pass filter suppresses the high frequency component of a signal and lets the low frequency component pass. It consists of a resistor and a capacitor in some particular configuration. The values of the resistor and capacitor determine the cutoff frequency, where the signal starts to attenuate. Beyond the cutoff frequency, the impedance of the capacitor increases and is attenuating the signal, whereas in lower frequencies, the capacitor tends to conduct the signal simply by charging up. RC low-pass filters are mainly mounted on audio applications as well as part of even broader electronic systems which filter their frequency content.

Within the PLL, the low pass filter is used to filter out the output from the phase detector that contains both the desired signal as well as noise, and also used as a stable source for providing a DC voltage to the loop filter. The LPF takes its input from the output of the phase detector; it can be implemented using RC filters, digital filters, or other techniques.

The dynamic properties of the PLL include capture range, lock range, transient response, and bandwidth. The “lock range” is defined as the frequency range within which the PLL circuit can track changes in the input frequency. The “capture range” is defined as the range in which the PLL can achieve phase lock.

As the bandwidth of the filter decreases, the response time increases and thus lessens the capture window. This does, however reduce unwanted noise and maintains stability of the loop after lock and minimizes signal loss. There are two common forms of passive low-pass filter used in PLL designs, which are often added with amplifiers to add gain.

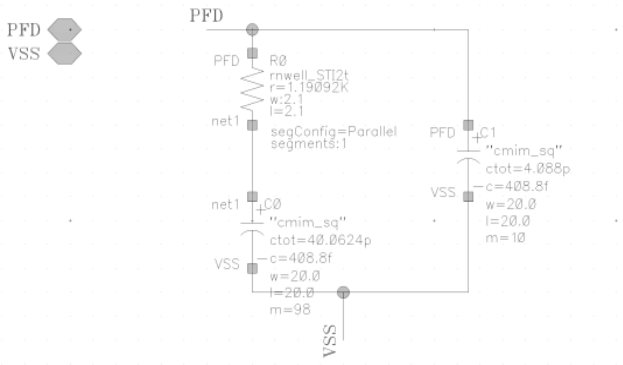

Figure 16: Designed LPF

Voltage Controlled Oscillator

A Voltage-Controlled Oscillator (VCO) is an electronic circuit which produces oscillations and these oscillations depend only on the input voltage provided to it. The requisite band of frequency required by the loop for its operation makes it possible to change the frequency of the oscillator. VCOs are used in different types of circuits in order to provide output signals where the output signals are a function of voltage variations at the input end.

For example, linear VCOs (LCVCOs) are typically used in most applications for frequency modulation synthesis. The output frequency here is the function of the control bias voltage. The exponential VCOs (EXPO VCOs) are further utilized because they have an exponential frequency response and can be operated in the correct manner to control voltage-controlled filters. The voltage-to-frequency converters (VFCs) are employed exclusively in frequency measurement and in applications that involve voltage-to-frequency conversion; that is, the input voltage is converted into its corresponding frequency. In addition, Digitally Controlled Oscillators (DCOs) combine analog oscillator circuits with digital control; hence, they lend themselves well to digital synthesis techniques. Ring oscillators, requiring inversion stages, generate square wave outputs for frequency division and clock generation.

In Phase-Locked Loops (PLLs), VCOs generate output signals whose frequency and phase can be controlled by the reference input and a loop filter. Since the VCO’s output is sinusoidal or non-sinusoidal in nature, its frequency is directly proportional to the input control voltage from the LPF of the PLL. Operational frequency of the VCO is quite near to the desired output frequency of the PLL that falls within kilohertz ranges to several gigahertz. The input voltage is furnished by the phase detector of the PLL to adjust the output frequency of the VCO.

The output frequency of a VCO is given by:

$$f_{out} = K \times V_{control}$$

where K is a constant defined as:

$$K = 1 / (2\pi(\sqrt{LC}))$$

For some circuits, the frequency can also be expressed as:

$$\text{Frequency} = (I_d / 2) \times N \times C_{total} \times V_{dd}$$

In fact, there are a number of different types of VCO circuits. On one end of this scale, they are nothing more than simple tank circuits comprised of capacitors, inductors, and resistors, while others take on much more complexity. Oscillating circuits can also be built with Op-Amps, multivibrators, transistors, and 555 timers. In reality, some ICs are also available, like the LM566 and LM567, intended for functioning as VCOs. So, to get a feel for the general idea of a VCO, it might be helpful to look at an example of an RC oscillator.

Although the mathematics involved in PLLs can be quite complex, the basic operation of how a PLL works is very simple. A basic phase-locked loop consists of three major components: a phase detector, a voltage-controlled oscillator, and a loop filter. In this scheme, the VCO signal and the reference signal are both fed to the phase detector. The output of the phase detector is fed to the loop filter; the filtered signal, in turn, changes the frequency of the VCO. The phase from the signal of the VCO is compared with the reference signal; the

difference in phase is output as an error voltage. This error signal is filtered through a low-pass filter and will remove high-frequency noise, controlling many aspects of the circuit. This filtered error voltage now serves as the control input to the VCO, which tunes its frequency down in order to reduce the phase difference between the two signals. Now, after lock-in, the VCO's frequency settles and matches that of the reference.

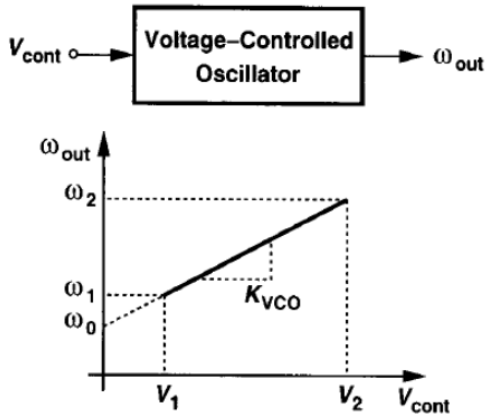

Figure 17: Transfer Function of VCO

Current Starved Voltage Controlled Oscillator (CSVCO): There are several architectures that can be used to design a VCO. For this purpose, we have chosen Current Starved VCO (CSVCO) for designing and analysis. It is preferred because the Current Starved architecture has lower sensitivity to supply voltage variations. The basic VCO structure is based on a Ring Oscillator and current mirrors in realizing the current-starved design.

The operation of the CSVCO bears a strong resemblance to the ring oscillator. In this circuit, MOSFETs M2 and M3 function as inverters, whereas M1 and M4 are current sources, as shown in Figure 18. That current flowing through M5 and M6 is then mirrored into each one of the inverter stages, where it is again under the control of the input voltage V_{in} VCO, thus "starving" the inverter stages of current.

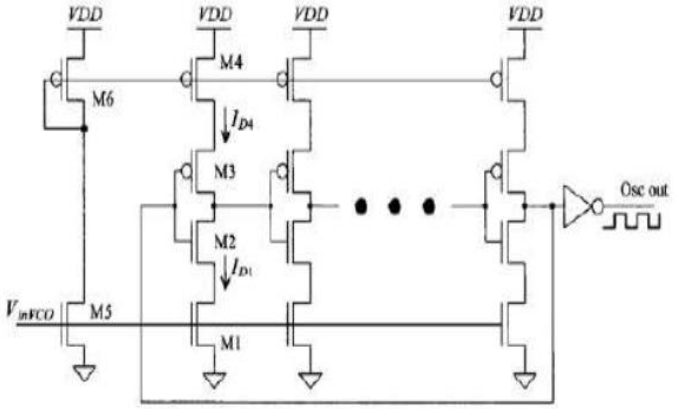

Figure 18: Basic implementation of CSVCO

Oscillation Frequency Calculation:

Total capacitance at the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in} \qquad (5.1)$$

$$C_{tot} = C'_{ox}(W_pL_p + W_nL_n) + (3/2)C'_{ox}(W_pL_p + W_nL_n) \qquad (5.2)$$

$$C_{tot} = (5/2)C'_{ox}(W_pL_p + W_nL_n) \qquad (5.3)$$

C_{out} and C_{in} simply represent the input and output capacitances of the inverter. The time taken to charge C_{tot} from zero to V_{SP} (switching point of the inverter) with constant current I_{D4} is given by:

$$t_1 = C_{tot}\,[V_{SP} / I_{D4}] \qquad (5.4)$$

While the time taken to discharge C_tot from V_DD to V_SP is given by:

$$t_2 = C_{tot}\,[(V_{DD}-V_{SP}) / I_{D4}] \qquad (5.5)$$

Since $I_{D1} = I_{D4} = I_D$, therefore

$$t_1 + t_2 = (C_{tot} \times V_{DD}) / I_D \qquad (5.6)$$

Hence, the oscillation frequency of a CSVCO with N (odd > 3) number of inverter stages is

$$f_{osc} = 1 / [N \times (t\_1 + t\_2)] = I_D / (N \times C_{tot} \times V_{DD}) \quad (5.7)$$

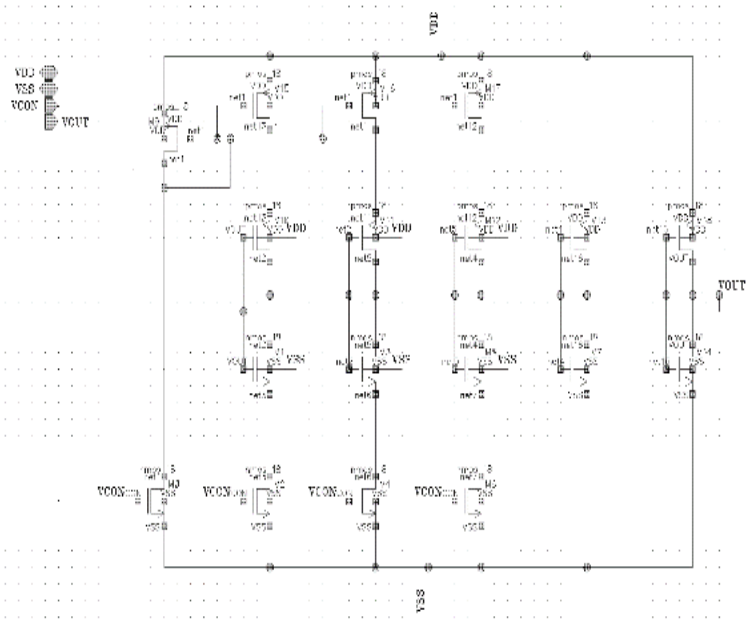

Figure 19: CSVCO Schematic

Table 1: CSVCO tuning

Control Voltage (in V)	Frequency Output (in Hz)
0.5	161.443 M
0.6	503.283 M
0.7	923.811 M
0.8	1.28009 G
0.9	1.57263 G
1.0	1.80369 G
1.1	1.97395 G
1.2	2.09325 G
1.3	2.17667 G
1.4	2.23411 G
1.5	2.27514 G
1.6	2.30558 G
1.7	2.32901 G
1.8	2.34736 G

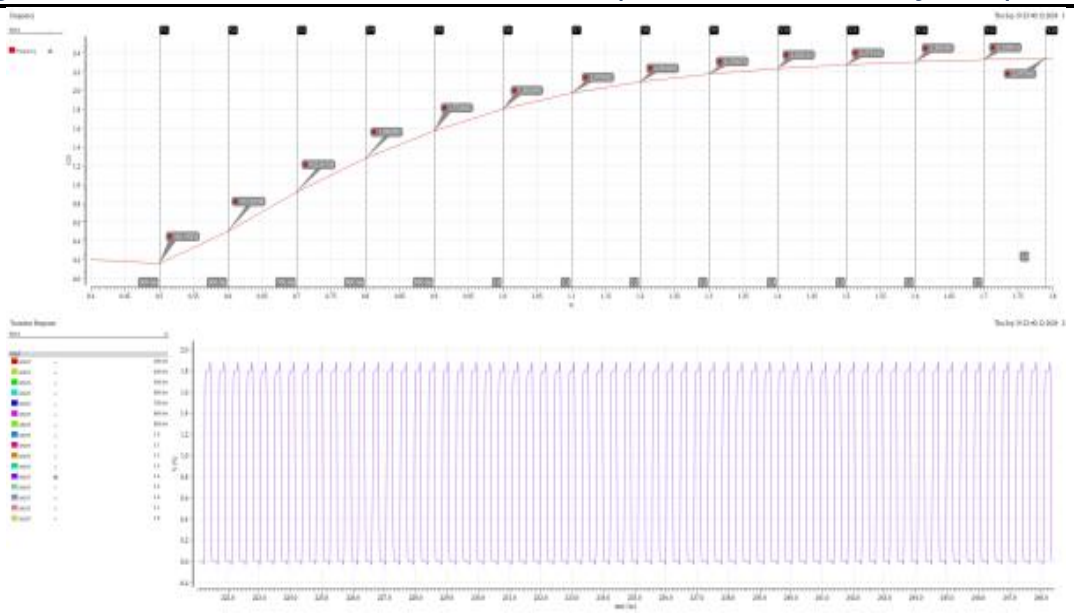

Figure 20: VCO Output

Frequency Divider

In an application where the range of frequency needs to be wide, a PLL requires a frequency divider for several critical reasons. First and foremost, the PLL functions by comparing the reference frequency F_{ref} with the feedback signal from the voltage-controlled oscillator (VCO) to get the frequency locking. Since the VCO's output could be many orders of magnitude greater than the reference frequency, the frequency divider scales the output of the VCO down to a value more comparable to the reference frequency. This can be expressed as $F_{divided} = F_{VCO}/N$. The VCO output can now be divided to equal the feedback frequency. This is how the PLL effectively locks its output at a desired multiple of the reference frequency, given by $F_{VCO} = N \times F_{ref}$.

Besides frequency matching, the frequency divider will help enable frequency synthesis, which is of significant use in creating a range of possible output frequencies. Output frequency is directly proportional to reference frequency in an integer-N PLL. Conversely, a fractional-N PLL facilitates finer granularity of frequency resolution by making use of fractional dividers; this facility makes it possible to produce non-integer multiples of F_{ref}. Such an ability is of significant utility in modern communication systems widely based on highly accurate frequency steps.

The flexibility in selecting the division factor allows the VCO to work efficiently and even at high frequencies where there may be an enhancement in the performance for the desired output.

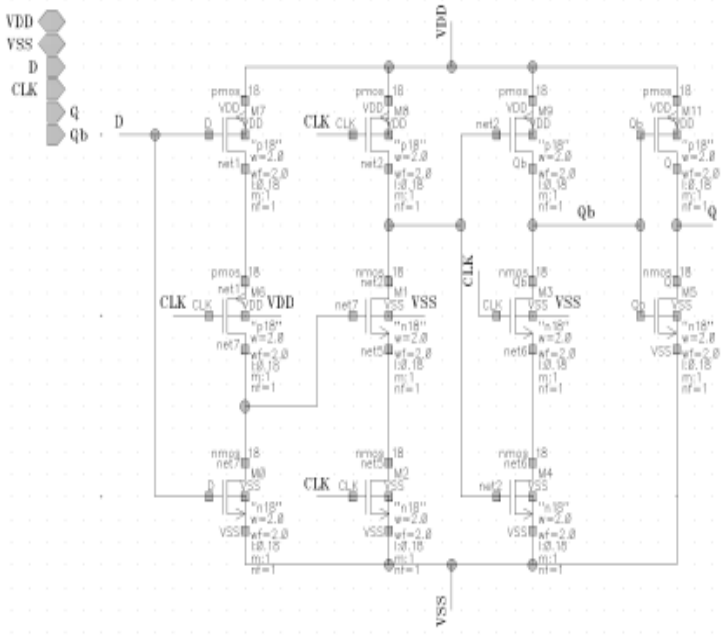

Figure 21: *TSPC DFF used for designing the frequency divider*

Another important advantage of including a frequency divider is its influence on phase noise. Lowering the VCO frequency decreases effective noise at the phase detector. Overall, it could lead to an even better phase

noise performance from the PLL, since high-frequency noise from the VCO would be much less audible after division.

Thus, the frequency divider is essential in designing a PLL since it enables matching feedback and reference frequencies, facilitates frequency synthesis, has support for wide frequency ranges, and improves phase noise characteristics. It provides the flexibility required to enable the VCO to operate at optimal frequencies while still building the output signal; that is why it is considered an essential factor in the functioning of PLLs

PLL

The PLL is simulated of a reference frequency of 100MHz, i.e, 10ns which serves as a solid ground to build upon a wide tuning range PLL. The feedback division ratio (N) is 4 in this case. The output frequency is around 394MHz.

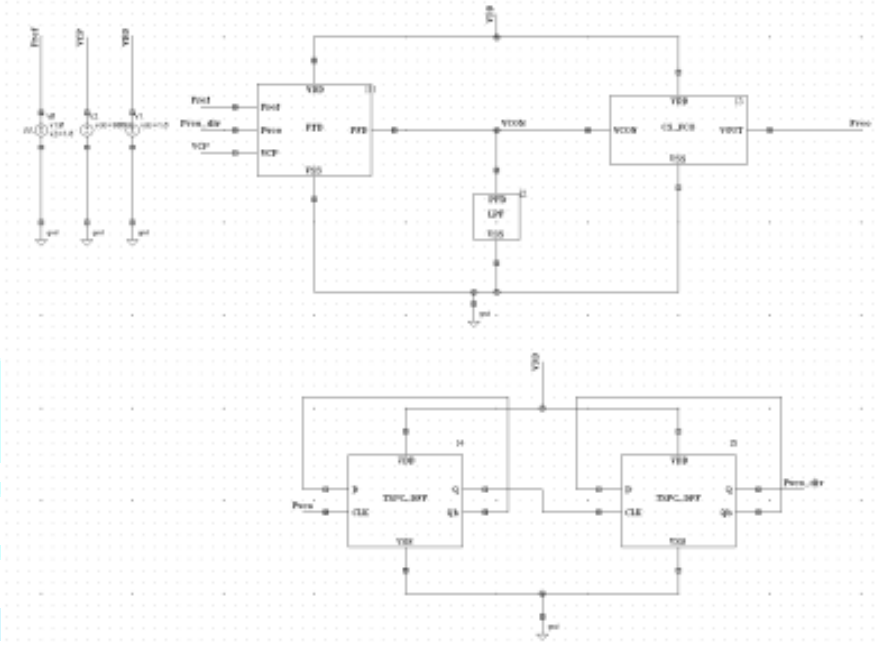

Figure 22: Implemented PLL

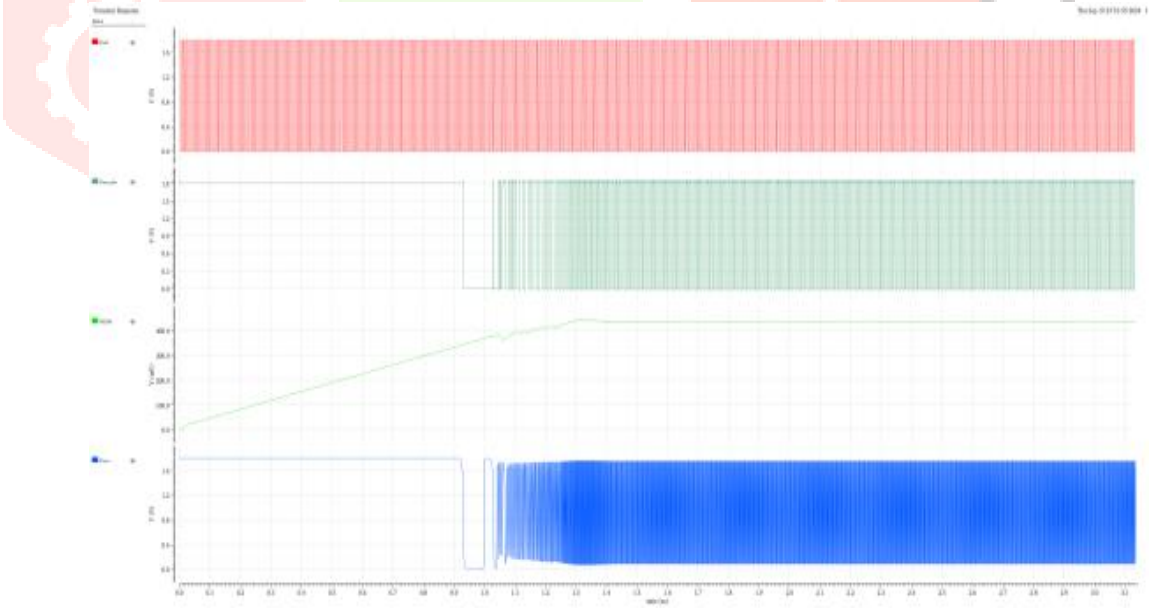

Figure 23: Output of PLL

VI. CONCLUSION

The schematics were rigged up using SCL-180nm PDK, re-ferring to standard design guidelines of PFDs. The simulation results are summarized as follows:

1) Standard PFD (Figure 2)consumes 11.6738µW of power.

2) Precharge PFD (Figure 6)consumes 5.25µW of power. 3) TSPC PFD (Figure 8)consumes 3.838µW of power.

The TSPC consumed the least amount of power compared to the other 2 designs.

Using the TSPC logic the PFD with charge pump was designed as shown previously in Figure 14. Following which the CSVCO and the Frequency divider were designed and the PLL was rigged up as in Figure 22. The output frequency for the loop was observed to be around 394 MHz for the division ratio of 4. The output is show in Figure 23.

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