IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Latch-Up Formation, Model And Modern Prevention Techniques

Rahul Nigam[1], Hare Ram Jha[2] and Kamini Vishwakarma[3]

[1]EC, Medicaps University, India
[2]EC, Medicaps University, India
[3]EC, Medicaps University, India

Abstract: This paper provides a view of the Latch-up problem in CMOS ICs. It shows how latch-up forms in CMOS ICs. In this paper, a Latch-up circuit model is displayed, and the circuit has been analyzed. This paper studies the causes of latch-ups and shows various methods to stop latch-ups. This paper provides a solution to the latch-up problem and conditions for stopping latch-up in CMOS ICs so that device failure can be avoided.

Index Terms: Latch-up, CMOS IC, SCR, Guard rings, ESD

1. INTRODUCTION

A chip that employs CMOS technology is known as a CMOS IC. This is the most widely used semiconductor technology for application specific integrated circuits (ASICs), Computer microprocessors, microcontrollers, and memory chips (RAM, ROM, EEPROM) are just a few of the numerous electrical devices that use CMOS integrated circuits. Due to several significant benefits, this technology is used in modern computer memory, CPUs, and cell phones. Both P channel and N channel MOS devices are used in this technique. An IC that has a short circuit between its power and ground rails, which results in high current and IC damage, is said to have a latch-up problem. Because parasitic PNP and NPN transistors create, latch-up, a phenomenon in CMOS transistors, develops a direct channel between the supply voltage and the ground. [1] A Silicon Controlled Rectifier (SCR, also called a thyristor, is a PNPN device used in power electronics) is like the structure created by this. These create a positive feedback loop, short circuit the ground and power, which eventually results in excessive current, and have the potential to permanently destroy the device. The parasitic SCR is in its blocking condition under normal bias, but latch-up may occur if it is subjected to an ionizing process or an abrupt shift in voltage. Device collapse or loss of state may result from this.

2. LITERATURE REVIEW

Latch-up problems have been a major issue with bulk CMOS ICs because of the PNPN structure form in CMOS. In conventional CMOS integrated circuit designs, the probability of latch-up triggering, a PNPN low impedance condition, is crucial. The issue has been extensively researched in relation to weaponry and space missions.

First, B. Estreich et al. show that the NPN current gain is mostly controlled by the base retarding field due to the doping level grade of the buried sublayer. A model has been made by them to directly depict the field improvement of the parasitic side PNPN current gain. [2] Gold doping, neutron irradiation, and changing the base transport factor with buried sublayers have all been used in sensible design to prevent latch-up occurrences, according to Ochoa et al. The propensity for VLSI consistency will increase parasitic activity sufficiently to make latch-up a more widespread problem. [3] J. E. Schroeder et al. explain a system of latch-up forestallment by replacing n in place of n+ material. They presented a graphical analysis that helps in understanding the latch-up phenomenon and provides a way to eliminate that state. [4]

K. W. Terrill et al. proposed a near system for precluding CMOS latch-up. By forming a p-buried sublayer beneath the CMOS bias, this system's mask-less boron implant lowers substrate resistance. [6] Morris W. provided descriptions of latch-up achieved by device and process modelling. He used ion implantation to create a low-resistance shunt sublayer, which has been found to be the most successful method for eliminating latch-up failures. [7]

To increase the latch-up immunity of CMOS ICs, H. W. Tsai and M. D. Ker suggested a technique called the active guard ring and affiliated circuit perpetration. By activating the electrostatic discharge (ESD) protection transistors with a new seeing circuit and an active buffer, the significant dimensional ESD bias can provide or admit redundant compensatory current to the positive or negative current disturbance at the time of the latch-up current test. [8] In a 0.18-µm technology, Z. H. Jiang and M. D. Ker successfully validated their innovative sensor circuit to prevent latch-up situations. Between the internal circuitry and the I/O pads, they install a hole/electron sensor that detects the latch-up detector current directed toward internal circuits. [9]

Latch-up may occur when CMOS circuitry malfunction. This could be a destructive hard failure, in which case the circuit is permanently lost, or a soft failure, in which case data or sense state is lost. Unless measures are made to improve latch-up robustness, device architectures become increasingly vulnerable to both failure modes as insulating extents decrease.

3. THEORY

A CMOS transistor made up of an NMOS and a PMOS device is depicted in Fig. 1. It contains parasitic transistor types Q1 and Q2. An n-well PMOS substrate forms the basis of the double emitter PNP transistor Q1. The PMOS source and drain outstation constitute two emitters, while the NMOS substrate (p-type) forms the collection. For Q2, the opposite is true. As previously mentioned, the two parasitic transistors function as an SCR by forming a positive feedback circle.

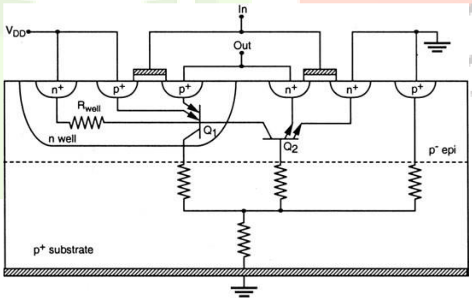

Fig. 1. Latch-up Generation in CMOS Device

The parasitic BJT production that results in latch-up is depicted in Fig. 1.

4. MODEL OF THE LATCH-UP CIRCUIT

The following requirements must be met to set up latch-up in any circuit [1].

1. For the structure remains latched, Q_2 and Q_1's device current gain product must be more than 1.

2. To start and maintain latch-up, both Q_2 and Q_1's emitter-base junctions need to be forward.

3. Both the source voltage and the source current drawn while latched must be supported by the voltage source.

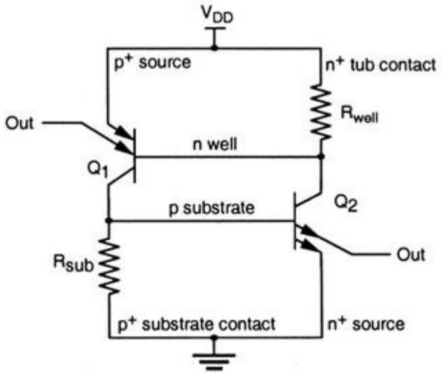

Fig. 2. A simplified schematic image of the parasitic devices in the CMOS inverter

An equivalent circuit of the parasitic devices Q_1 and Q_2 in the CMOS inverter display in Fig. 2. The actual resistance that exists between the substrate contact and the NPN base and the well contact and the PNP base is represented by the shunting resistors Rwell and Rsub. Both transistors' collector current is made up of rear leakage current unless an external disturbance touches off the SCR. At the base junction, transistor Q_2 receives the collector current of transistor Q_1 ($I_{C1} = \beta_1 * I_{B1}$). Thus, transistor Q_2's collector current ($I_{C2} = \beta_2 * I_{B2}$) functions as an input current to transistor Q_1 at the base junction. The total current gain in this loop increases because of the feedback between the Q_1 and Q_2 transistors.

$\beta_1 * \beta_2$ is the total current gain that results from the SCR device loop.

Current disturbance * gain equals the total current in a single circle.

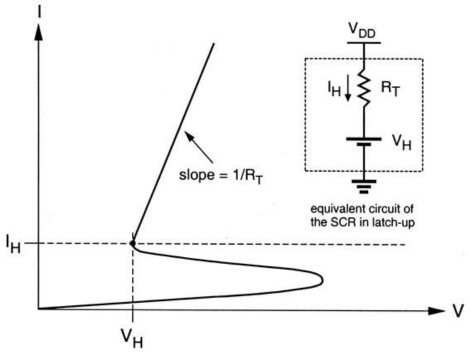

Fig. 3. An SCR Current Voltage Characteristic

Next,

Latch-up causes the voltage to drop across the SCR

V_H holding voltage = $V_{BE1,\,SAT} + V_{CE2,\,SAT}$

$= V_{BE2,\,SAT} + V_{CE1,\,SAT}$

I_H is holding current, then

The state is low impedance if $I > I_H$, R_T total parasitic R in the current path [11].

Even so, if $\beta_1 * \beta_2 >= 1$, both transistors will conduct a significant current once the driving concern is removed. In the end, this current will become so high that it could harm the electronic device.

Fig. 2 [5] illustrates the explosive dependence of the holding current on R_{well} and R_{sub}. The physical explanation is obvious: When R_{well} or R_{sub} is low, an advanced current must flow to keep the base-emitter junctions forward biased. Fig. 2 is a "strong" layout because the substrate and well contacts are between the devices; if they were, say, on the opposite sides of the devices, R_{well} and R_{sub} would also rise and the circuit would become more sensitive.

5. CAUSES OF LATCH-UP

The main causes of Latch-up are as follows: -

1. The COMS process is more complicated than normal NMOS alone since NMOS and PMOS transistors must be manufactured simultaneously on the same chip.
2. The PMOS transistor requires an N-substrate from the COMS process, and vice versa.
3. This can be accomplished by constructing an n-type well and a p-type wafer, or the other way around.
4. Nevertheless, the proximity of the NMOS and PMOS transistors may influence the configuration of two parasitic BJTs, leading to a latch-up issue.
5. A high V_{DD} leads slew rate at the start (relegation currents and dynamic recovery if the slew rate is not very high).
6. Due to transmission line impedance mismatches, I/O signals fluctuate a lot above power supply or below V_{SS}.
7. ESD stress (substrate or well minority carrier injection setup device)
8. Unexpected interruptions in cars (caused by multiple drivers switching at the same time) [10]

6. LATCH-UP PREVENTION TECHNIQUES

Regarding the latch-up problem, the next two elements are crucial:

1. $\beta_1 * \beta_2 > 1$

2. High resistance of n-well and p-substrate

To prevent latch-up, a high resistance is placed in the path to forcefully hold down the current and make $\beta_1 * \beta_2 < 1$.

The following two methods can be used to accomplish this:

1. PMOS and NMOS transistors are encased in a separating oxide layer. This eliminates the SCR structure's parasitic effect.

2. The circuitry of the latch-up protection technology, which turns the device off when latch-up is detected. [10]

The following are some additional well-liked latch-up protection techniques.

1. The Guard ring
2. The Well connections
3. The Oxide layer insulation
4. The Epitaxial layer
5. The Retrograde well doping
6. Combination of epitaxial layer and retrograde well impurities
7. SOI Technology
8. ESD protection pathways

6.1 THE GUARD RING

If V_{out} falls below the V_{SS}, the parasitic diode between the drain and the p-substrate of NMOS comes forward bias, and electrons from the drain begin to edge in from the substrate and be collected by the PMOS body. As a result of the electron input, the current travels in the opposite direction. This, as seen in Fig. 1, ultimately activates the Q_1 transistor. As seen in Fig. 4, two sets of n-implants in n-wells and p-implants on p-substrate were inserted between NMOS and NMOS to break this link. These will gather the electrons that are fitted from the NMOS drain and prevent current from flowing from the NMOS drain to the PMOS body. It stops the Q_1 BJT from being driven.

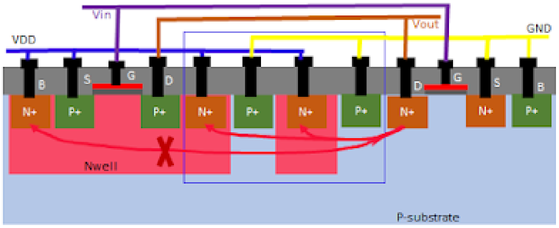

Fig. 4. The Guard Ring

Additionally, if the V_{out} rises above the V_{DD}, the PMOS drain begins to edge in n-well holes before being collected by the NMOS body. This resulted in the Q_2 transistor drive. In this approach by guard ring latch-up development can be avoid.

6.2 THE WELL CONNNECTIONS

The n-well to supply V_{DD} and p-sub to GND V_{SS} must be reached by these well contact cells to stop the latch-up. Fig. 5 displays the selection of contactless cells, and Fig. 6 displays the arrangement of both contactless standard cells and well contact cells.

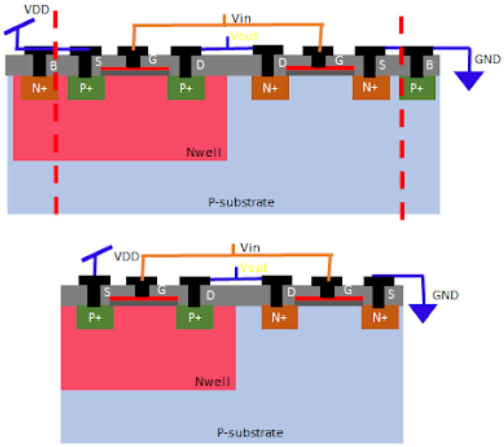

Fig. 5. View of contact and contactless cell

The well contact cells are positioned in the standard cell row at regular intervals in accordance with the maximum distance rule defined in the technology library.

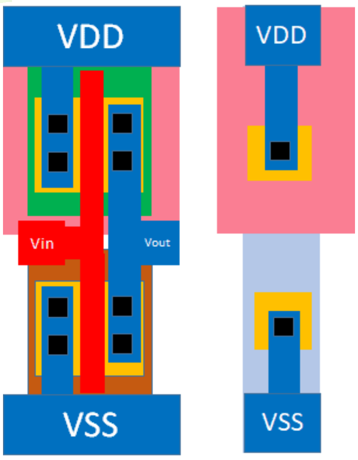

Fig. 6. Layout of contactless cell and well contact cell

6.3 THE OXIDE LAYER INSULATION

This technique uses the buried oxide and oxide layer to isolate NMOS and PMOS. To divide the n-well and p-substrate, a vertical buried oxide is made deep outside, and later, perpendicular oxide layers are formed and joined together. Since the oxide layers are solitary in nature, they prevent the PNPN device from setting up. Fig. 7 displays a variety of oxide layer insulation.

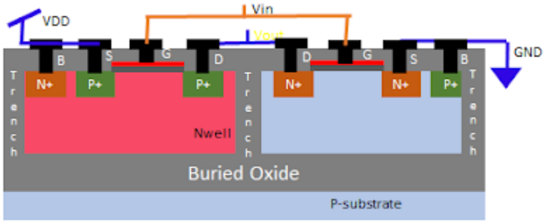

Fig. 7. view of an isolation

6.4 THE EPITAXIAL LAYER

This method made use of a low doping deposit over the P-substrate and a p-type epitaxial layer (referred to as P-). To prevent latch-up triggering, the P-epitaxial layer provides a low impedance channel for minority carriers. Another name for this methodology is P- on P+. Figure 8 displays a cross-sectional image of the epitaxial layer.

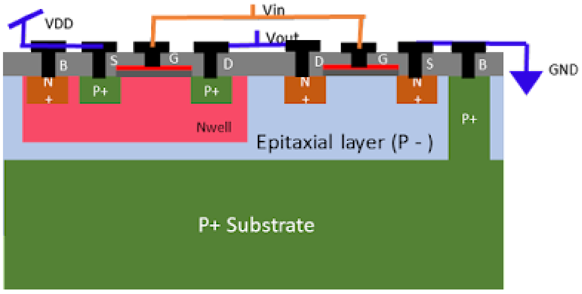

Fig. 8. Epitaxial layer cross-section image of CMOS

The epitaxy layer is extremely difficult to deposit using this procedure, which is its only drawback. The epitaxial wafer can likewise be used in this way.

6.5 THE RETROGRADE WELL DOPING

In common n- well doping operation, the doping attention is uppermost at the shell and it decreases as the depth of well increases. But in the retrograde well doping procedure, there's veritably exact control of doping immersion over the depth and we've peak doping immersion at deep inside the n- well, not at the shell. A doping profile of normal doping and retrograde well doping is shown in Fig. 9.

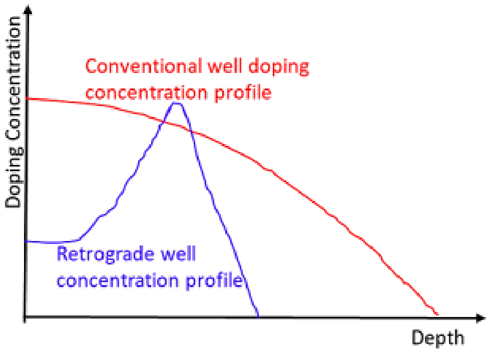

Fig. 9. doping concentration of retrograde well impurity

The doping focus is highest at the shell in a typical n-well doping operation and diminishes with increasing well depth. However, the retrograde well doping process allows for incredibly precise control over doping immersion throughout the depth, with peak doping immersion occurring deep into the n-well rather than at the shell. Fig. 9 displays a doping profile of retrograde well doping and normal doping.

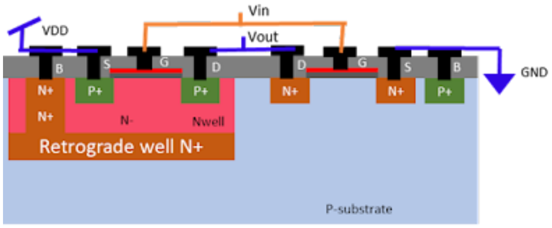

Fig. 10. Retrograde well-doped CMOS

6.6 COMBINATION OF THE EPITAXIAL LAYER AND RETROGRADE WELL IMPURITIES

Although the procedure is a little complicated, we can stop the latch-up problem by combining the epitaxial position and retrograde well impurity, which is also a very successful method.

6.7 SOI TECHNOLOGY

The parasitic BJT configuration is stopped by an oxide layer that sits on top of the source-drain doping in SOI (Silicon on Insulator) technology. Thus, the latch-up issue is resolved via SOI technology. Fig. 11 displays a view of SOI technology.

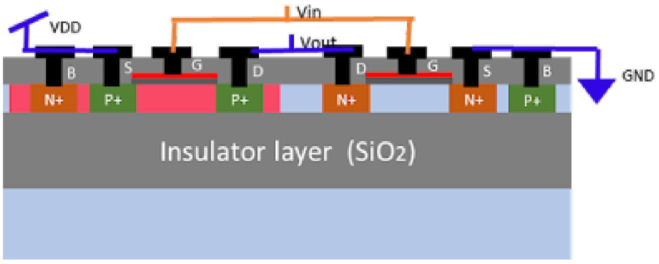

Fig. 11. SOI Technology

7. CONCLUSION

We research about the dependability issue known as latch-up that plagues CMOS processes. It may be crucial to the design or activated by voltage spikes on I/O pads that could further bias PN junctions to which it was coupled. It behaved in circuits by either malfunctioning or using excessive power. However, there are methods for preventing latch-up in CMOS technology. Doping can lower n-well and p-substrate resistance, but it will significantly impair device performance. However, we can prevent the latch-up problem and reduce the gains of parasitic BJT (β). The benefits and drawbacks of each approach are examined.

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