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FPGA-BASED HIGH-SPEED AND DYNAMIC ARCHITECTURE DESIGN FOR COLOR CONVERSION IN REAL-TIME COMPUTING

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Abstract: FPGA implementation of different image processing methods has become necessary due to the growing need for video processing on hardware. A significant amount of research is being conducted in the field of image processing and video processing using FPGA. The paper discusses two implementation blocks, namely picture block generation and RGB to YCbCr and YCbCr to RGB conversion. The design has demonstrated that it is effective for high definition (HD) video sequences with frame sizes of 1920 x 1080. The experimental results show that the implemented hardware architecture performs well while converting color spaces from RGB to YCbCr. Among the logic devices known as programmable logic devices (PLDs) is a subset called FPGAs. Their composition consists of a grid of interconnected programmable logic blocks that can be set up "in the field" to connect with other logic blocks to carry out different types of digital operations. While the increased cost of individual FPGAs is not as significant and where designing and producing a custom circuit would not be practical, FPGAs are frequently employed in limited (low) quantity manufacture of custom-made items and in research and development. The versatility, high signal processing speed, and parallel processing capabilities of FPGAs are advantageous in the automotive, aerospace, telecommunications, and industrial domains. It also offers the advantages of being fast, simple, and little in size. Both bocks are intended for use on commercial field programmable gate array (FPGA) devices.

Keywords: Image Processing, Field Programmable Gate Array (FPGA), Color Space Conversion, and Xilinx system generator are all terms used to describe image processing.

1. Introduction

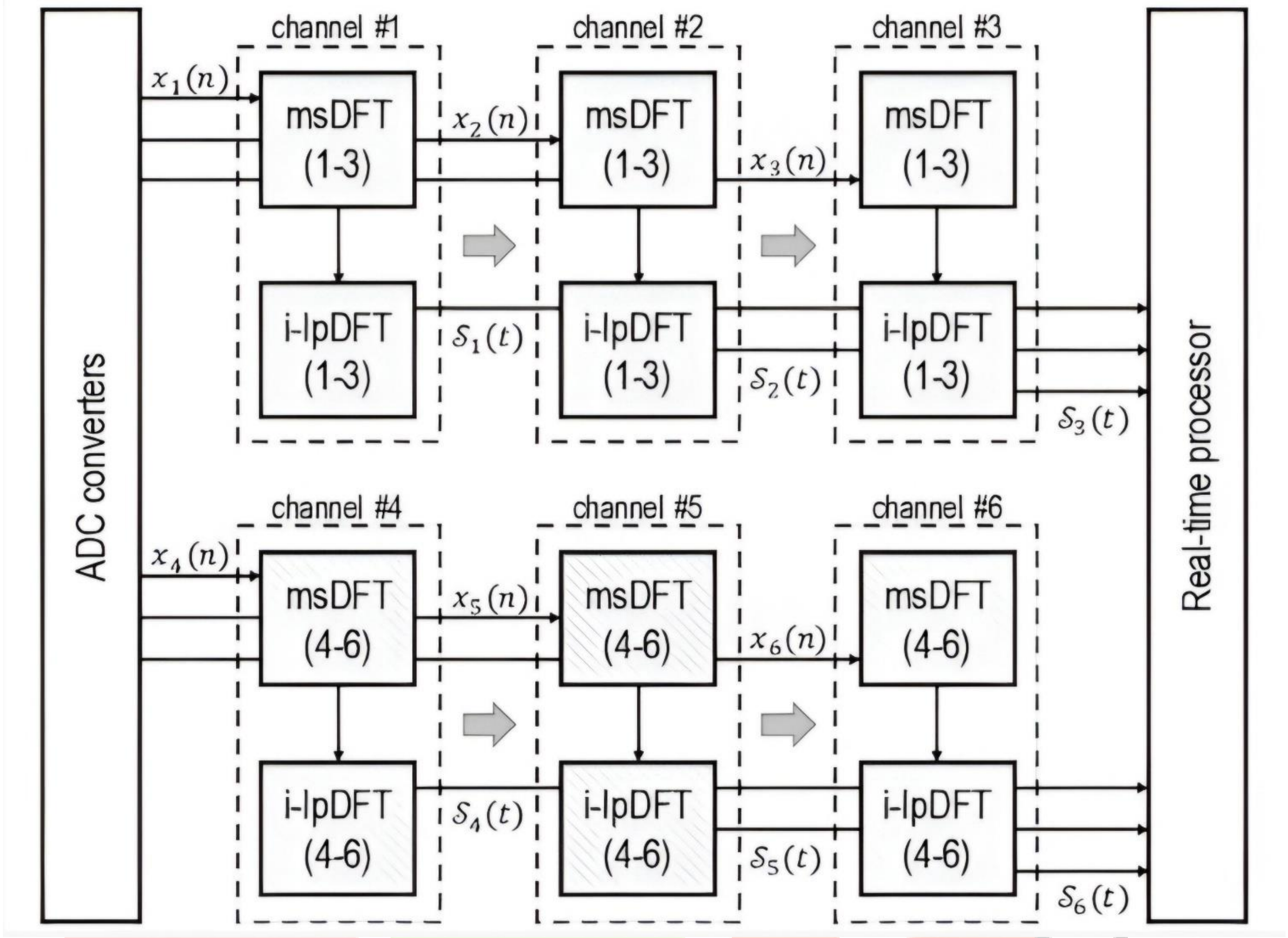
Because of the increased demand for enhanced security, intelligent surveillance systems are becoming increasingly popular[1,2]. Color space conversion has become extremely significant in video processing and transmission technologies; in general, transmitting images in RGB color space is impractical due to the huge bandwidths required. The human eye is more sensitive to changes in brightness than it is to changes in color. As a result, if luminance-chrominance color space is employed for color image transmission, data storage and bandwidth can be lowered, at the expense of overlooking very small or nearly unnoticed color change information. YCbCr is a color model that is hardware-oriented. When we process video in YCbCr color space, we may achieve very high compression ratios and transmission rates; therefore, in most image or video compression applications (for example, JPEG and MPEG), we will usually need to employ the transformation between RGB and YCbCr color space. Color space converter (CSC) hardware is significantly more efficient than software implementation. As a result, we can boost our system's performance by building a hardware accelerator (HA) for Conversion of color spaces. However, in terms of delay or hardware costs, multiplication in a general-purpose processor or a bespoke hardware implementation is often an expensive operation. When we convert CSC from RGB to YCbCr, we face two quandaries in hardware circuit design.

However, as the demand grows, more systems with higher performance and shorter execution times are required. FPGAs, or Field-Programmable Gate Arrays, are circuits comprised of logical blocks that can be reconfigured as many times as necessary to debug their functionality. They communicate with one another via entrance/exit terminals via fences known as communication channels. FPGAs have the same size and speed as ASICs, but they are more flexible, have a quicker design cycle, and have superior performance due to parallelism [1,2]. To comply with the ITU-R BT.601-5 standard, the DIGILENT VDEC-1 card digitizer (handles analog to digital conversion) delivers the video signal in digital format of the YCbCr color model; these signals are then transformed to the RGB color model and can be interpreted by a monitor [5,6].

This article is organized as follows: in section 2, the model transfer equations from YCbCr to RGB, as specified by ITU-R standard BT.601-5, are presented. In Section 3 will give a proposed architecture for color system conversion for the creation of a digital conversion system between each color model (YCbCr and RGB). In section 4, the results for the suggested architecture for color system conversion are shown; the results will be bought numbers obtained by the digital design in the FPGA and shown in section 2. Finally, the conclusions reached during the production of this study.
Recent developments in areas like image and video processing, augmented reality, and machine learning have increased demand for high-speed processing in real-time computer applications. Color conversion is a crucial process in these fields that entails converting image data between different color spaces for a range of uses, such as image enhancement, video transmission, and display rendering.
Because of its inherent reconfigurability and parallel processing capabilities, Field-Programmable Gate Arrays (FPGAs) have become a reliable choice for developing high-speed designs. Through the utilization of FPGA technology, designers are able to produce customized hardware that expedites intricate algorithms, yielding noteworthy enhancements in performance in comparison to conventional CPU-based systems.

The design of an FPGA-based architecture especially suited for dynamic, fast color conversion in real-time computer systems is examined in this study. Our goal is to efficiently handle large amounts of image data by minimizing latency and optimizing the design for parallel processing. Our methodology entails the creation of modular components that are scalable and able to conform to different color spaces and processing specifications, guaranteeing flexibility in a range of applications.

We show how FPGA-based architectures can effectively address the difficulties involved in real-time color conversion, opening the door to improved performance in multimedia processing jobs, through thorough study and implementation. This work paves the way for further advancements in real-time



computing while also highlighting the benefits of employing FPGAs for this purpose.

2. Color System Conversion

Color space is the mathematical representation of a color set. As the most popular choice in display graphics, RGB is the most commonly utilized standard for picture presentation. Using the RGB[1,11] combination, any color can be generated. However, it cannot be utilized for video processing because the frame buffer requires pixel depth and display resolution for each RGB component. This can be demonstrated with an example: suppose the intensity of the given input image needs to be changed. In this process, we must create a unit that can function independently on all three components, regenerate each RGB value, and rewrite the new values on the frame buffer, as illustrated in Figure 1. This procedure often takes longer than other color spaces, such as YCbCr, where we just need to work on the intensity rather than the color component, making the work faster and easier with fewer computational complications required.

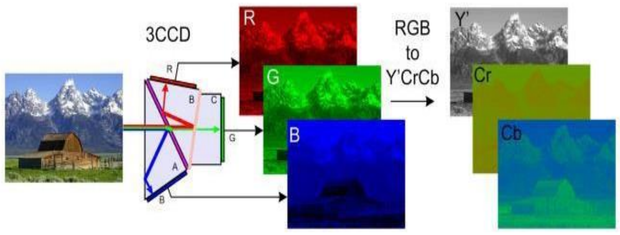


Figure 1: RGB to YCbCr representation

The color space standard used for real-time video and picture is YCbCr. It is widely utilized in all video standards, including PAL, NTSC, SECAM, and composite color video. Only the Y component is used in black and white. Additional Cb and Cr components were also added. As previously stated, RGB is commonly utilized for all display unit data available to the user, therefore it is absolutely important to convert RGB to YCbCr format. The equations shown below are used to convert images from one format to another. The transition from the RGB color space (red, green, blue) to the YCbCr color space (luminance, chrominance) attempts to increase the efficiency of the JPEG compression process. Indeed, the human eye is not particularly sensitive to changes in chrominance. The brightness channel appears to be fairly comparable to the original image's grayscale version. Cb is prominent in images where the blue color dominates, such as those taken from the sky. Cr is dominant when the image is obtained from locations where reddish colors dominate, while both Cb and Cr factors are weak when the green color is dominant. [7,8] Figure 2 depicts the color difference in different channels as well as the difference between RGB and YCbCr.

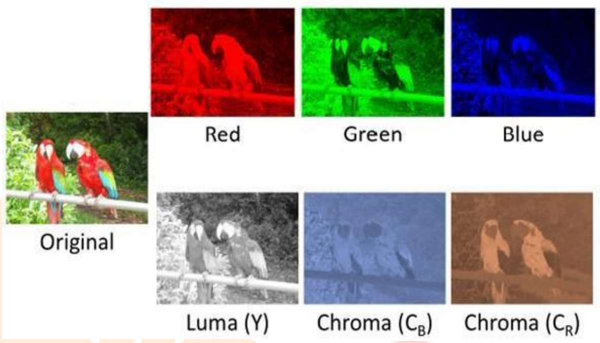
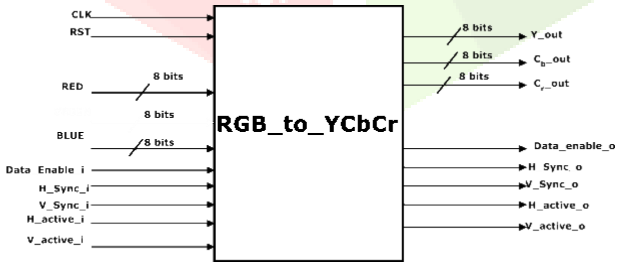


Fig. 2: Difference between RGB and YcbCr

3. Hardware Implementation of the ProposedCSC architecture

This section describes hardware architectures built for RGB-YCbCr and YCbCr-RGB color space conversion. The color space conversion algorithm was used to construct the architecture.



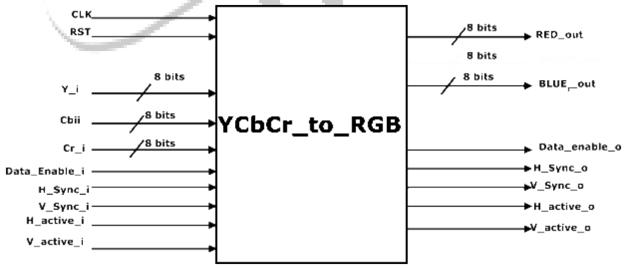


Fig. 3: RGB to YCbCr Block

Fig. 4: RGB to YCbCr Block

The IP block Color space conversion has two modules: RGB to YCbCr and YCbCr to RGB. The RGB to YCbCr Color Space Converter IP module implements the equations required to convert 24-bit RGB color samples to 24-bit YCbCr color samples. The YCbCr to RGB Color Conversion The Space Converter IP module transforms RGB to YCbCr and vice versa. Both converters employ the 4:4:4 sampling format. Both modules accept data enable, horizontal, and vertical sync signals as inputs and pipe them to match the conversion video data outputs. The floating point constants are scaled by multiplying them by 215 = 32768 to convert them to integer multiplication. The output is then divided by the scaling factor 215 = 32768 after the preceding equations are computed. Figure 3 depicts the top level signal diagram for the RGB-YCbCr color space conversion module. Figure 4 depicts the detailed hardware architecture for RGB to YCbCr and YCbCr to RGB color space conversion. Figure 5 depicts a direct mapping of the three equations listed above. This conversion is accomplished by using floating-point multipliers and summing circuits to conduct digital multiplication and addition.

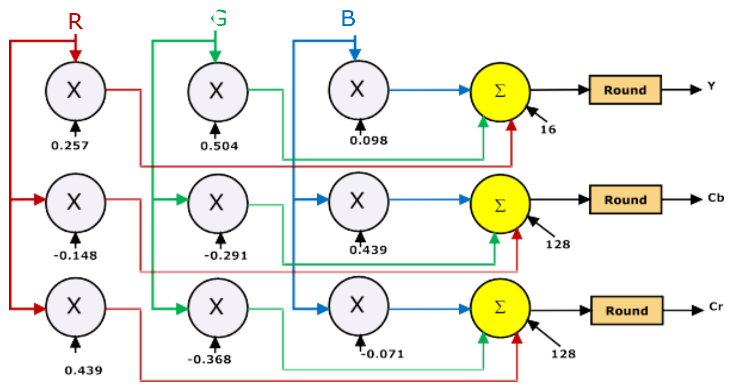
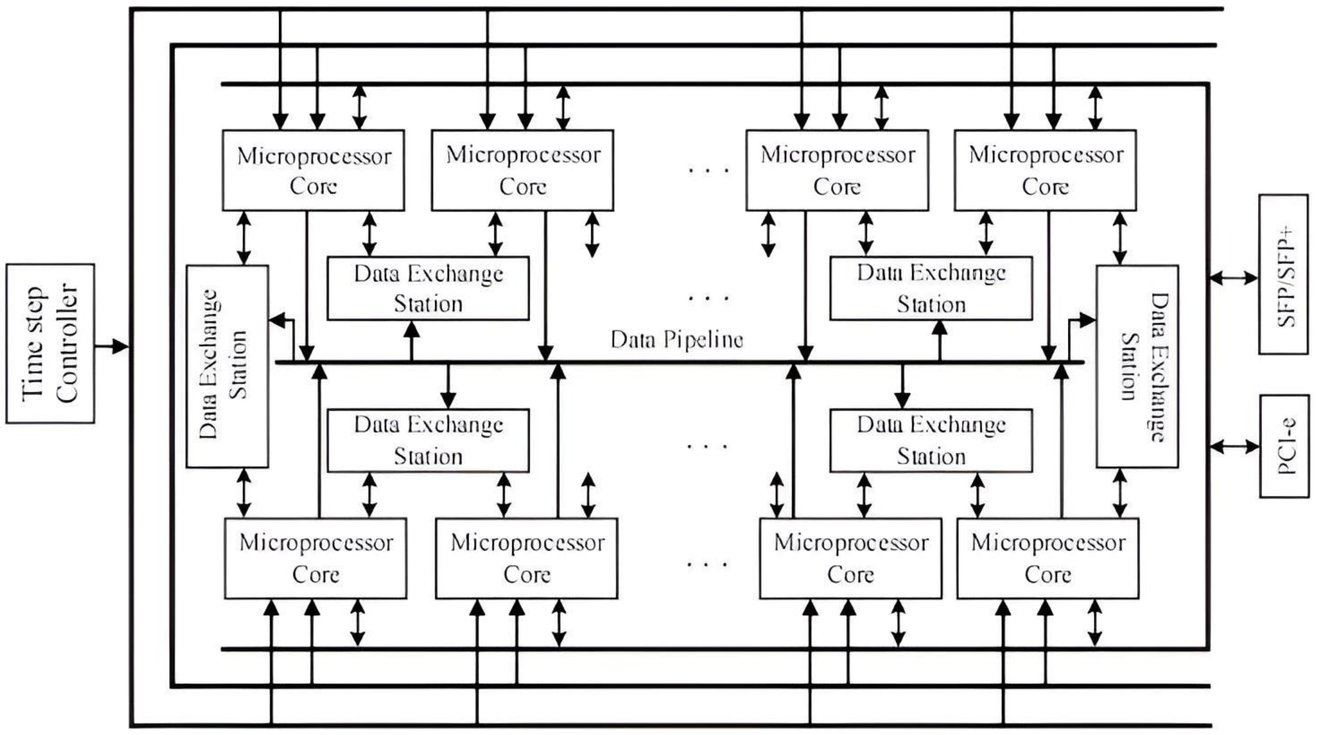


Fig. 5: General block diagram for RGB to YCbCr.

Color space conversion hardware implementation begins with Matlab verification and is followed by hardware architectural development, VHDL coding, logic synthesis, place and route, and FPGA implementation. First, we implement an RGB to YCbCr converter on an FPGA. The RGB to YCbCr converter module is designed using Eqns. (1) to (3). Comparator, subtractor, divider, adder, and hue selection are the hardware components utilized in RGB to YCbCr conversion.To speed up the conversion process, the VHDL codes produced for these modules are pipelined and processed in parallel [10]. The divider block is the most complicated module in this conversion process. The divider used in the conversion process, on the other hand, is extremely efficient. Finally, the hue selection block selects the computed individual hue values Color space conversion hardware implementation begins with Matlab verification and is followed by hardware architectural development, VHDL coding, logic synthesis, place and route, and FPGA implementation. First, we implement an RGB to YCbCr converter on an FPGA. The RGB to YCbCr converter module is designed using Eqns. (1) to (3). Comparator, subtractor, divider, adder, and hue selection are the hardware components utilized in RGB to YCbCr conversion.



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4 Simulation:

The proposed FPGA implementation of image color space conversion has been coded in Matlab and tested first to guarantee that the color space conversion developed works properly. The results of the testing were excellent. Following that, the entire design was programmed in VHDL and simulated using ISE 14.1. Xilinx 14.1 is used for synthesis, placement and routing, and bit file production. Figure 6 depicts the ModelSim waveform findings for RGB-YCbCr and RGB-YCbCr conversion.

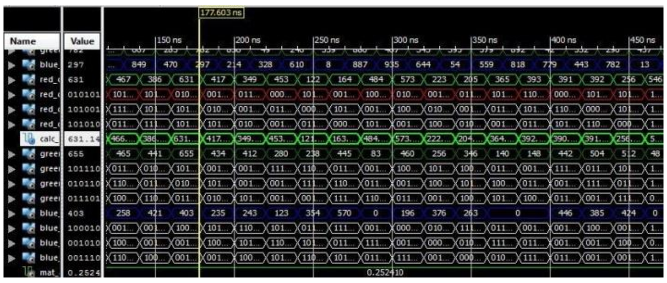

Fig. 6: Waveforms for RGB to YCbCr and YCbCr to RGB Conversion

Color System Conversion with Xilinx SystemGenerator:

System Generator is a component of the ISE® Design Suite that provides the Xilinx DSP Block set for application-specific design, including adders, multipliers, registers, filters, and memories. These blocks make use of the Xilinx IP core generators to produce optimized results for the chosen device. When using System Generator [10,11,11], no prior familiarity with Xilinx FPGAs or RTL design approaches is required.

The Xilinx CORE Generator system creates and provides parameterizable cores for Xilinx FPGAs. It is used to develop high-density Xilinx FPGA devices, achieving great performance outcomes while lowering design time. The ISE Xilinx Foundation includes the CORE Generator, which includes a range of core memories and storage elements, math functions, DSP functions, and a variety of basic elements. Elements. The Xilinx Core Generator14.2 generates the RGB to YCbCr and YCbCr to RGB cores, which are tuned for 8-bit input data and 8-bit output data. FPGA Color-space conversion implementation The IP-cores shown in Fig. 7 are made up of two IP-cores: The IP-core RGB2YCrCb transforms RGB inputs to YCrCb, and the IP-core YCrCb2RGB translates YCbCr signals back to RGB.

5 Synthesis Results:

Implementation of the proposed design was made on Xilinx Zynq and Virtex Family Platforms: XC7Z020 and XC7VX330T devices. We have used the Xilinx ISE tools version 14.1 . The synthesis results of the architecture is shown in Table 1 and Table 2.

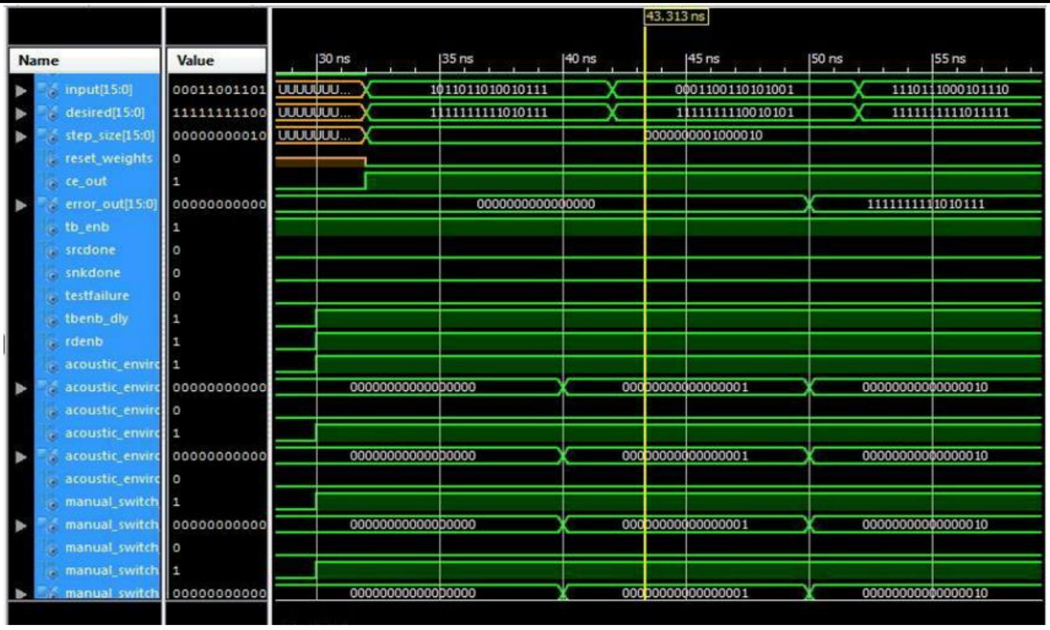

Table 1: RGB to YCbCr Color Space Conversion Implementation using Xilinx FPGA Device

Parameter	xc7z020- 2clg484		xc7vx330t-2ffg1157	
Logic Utilization	Used	Available	Used	Available
Number of Slice Registers	172	109800	172	418000
Number of Slice LUTs	172	59200	172	214000
Number of fully used LUT-FF pairs	156	123	156	129
Number of bonded IOBs	69	209	69	600
Number of BUFG/BUFGCTRLs	1	32	1	34
Number of DSP48E1s	4	220	4	1120
Frequency (MHz)	438.702		492.017	

Table 2: YCbCr to RGB Color Space Conversion Implementation using Xilinx FPGA Device

Parameter	xc7z020- 2clg484		xc7vx330t-2ffg1157	
Logic Utilization	Used	Available	Used	Available
Number of Slice Registers	120	106400	120	408000
Number of Slice LUTs	99	53200	99	204000
Number of fully used LUT-FF pairs	99	120	99	120
Number of bonded IOBs	63	200	63	600
Number of BUFG/BUFGCTRLs	1	32	1	32
Number of DSP48E1s	4	220	4	1120
Frequency (MHz)	441.562		494.148	

The RGB to YCbCr and YCbCr to RGB conversions are straightforward and accommodate a wide range of frequencies. However, they need a great number of resources. Because each output channel is a linear mixture of the inputs, forward conversion necessitates 9 multipliers and backward conversion necessitates 5. Because of the difference in the number of multipliers, the RGB2YcbCr conversion can function at almost 438 MHz, whereas the YcbCrtoRGB conversion can only support around 441 MHz. Tables 3 and 4 indicate the utilization rates. Tables 3 and 4 show the frame rate required to decode various FHD frames.

Table 3: Frame Rate control for RGB to YCbCr conversion

MODE-1

Max frequency : 438**MHz**		
Resolution	Pixel per frames	Maximum Frame Rate
1920x1080	2073600	232,92 FPS
1440x900	1296000	372,71 FPS
1024x1024	1048576	460,58 FPS
1280x720	921600	524,04 FPS
1024x768	786432	614,21 FPS
640x480	307200	1572,30FPS
512x512	262144	1842,48FPS

MODE-2

Max frequency : 441 **252 MHz**		
Resolution	Pixel per frames	Maximum Frame Rate
1920x1080	2073600	212,62 FPS
1440x900	1296000	340,2 FPS
1024x1024	1048576	420,52 FPS
1280x720	921600	478,45 FPS
1024x768	786432	560,7 FPS
640x480	307200	1435,52 FPS
512x512	262144	1682,27 FPS

Conclusion :

This article proposed efficient architectures for FPGA/ASIC implementation of RGB-HSV and RGB-YCbCr color space conversion. picture compression, picture augmentation, and segmentation are some of the potential applications of the suggested techniques. Pipelining and parallel processing techniques are used to accelerate the conversion process. The Verilog code created for the entire system is RTL compliant and suitable for ASIC construction. This paper's implementation was realized using a Xilinx XC7Z020-2clg484 FPGA device. When compared to other current implementations, the experimental results suggest that the proposed color space conversion algorithms work better. As a result, the developed CSC architecture can encode 232 video frames/s of high-definition TV with 1,920 pixels. High-speed real-time picture compression techniques are required.

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