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Redundant Transition Free Low Power TSPC Dual-Edge-Triggering Flip-Flop With Clocked Single Transistor

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ABSTRACT--- In the age of artificial intelligence (AI) and graphics processing units (GPUs), the flip-flop (FF) has emerged as one of the processor's most power- hungry elements. A unique single- phase-clock dual edge triggering (DET) FF employing a single transistor clocked (STC) buffer (STCB) is suggested as a solution to this problem. The clock redundant transitions (RTs) and internal RTs present in previous DET designs are eliminated entirely by the STCB's use of a single- clocked transistor in the data sampling path. The suggested STC-DET beats the previous state-of-the-art low-power DET in power consumption by 14% and 9.5%, at 0.4 and 0.8 V, respectively, when running at 10% switching activity, as shown by post-layout simulations in 22 nm fully depleted silicon on insulator (FD-SOI) CMOS. Among the DETs, it also attains the lowest power-delay-product (PDP).

Keywords**:** Flip-Flop, Dual-EdgeTriggered, Low Power, TSPC (TrueSingle-PhaseClock), Redundant-Transition-Free Clocked Single Transistor.

I. INTRODUCTION

Two-edge the system clock signal is one of the main dynamic power consumers in computing and consumer electronics products, accounting for between 30% and 70% of the overall dynamic (switching) power consumption .Clock gating is the most common of several methods that have been devised to lower the dynamic power. A logic unit's underlying sequential elements typically receive the clock signal when it is clocked, regardless of whether or not its data will toggle in the subsequent cycle
.Clock gating involves ANDing the clock signals with enabling signals that have been specifically stated [1].
The schematic of the receiver reveals the several blocks that, in a sequential fashion, enhance the signal-to-noise ratio [2]. A low- noise amplifier is an electrical device that may boost weak signals while preventing them from being distorted by outside noise. Reducing amplifier noise is an LNA's primary purpose. One of its many uses is to improve signal-to-noise ratios by amplifying weak signals within a certain frequency range while attenuating incoming noise signals [3].

II. LITERATURESURVEY

"Auto gated flip-flops as the basis for a look ahead clock gating "Suggest the XOR free clock gating technique. Integrate clock gating strategies that are state-based and toggling- based. Inefficient use of resources in clock gating depending on input data toggling. A crucial and pricey part of XOR gates that detects input toggling. The input data toggling method's gating logic is limited. In efficient use of resources was noted in the gating logic."Explicit pulsed dual edge triggered sense amplifier flip-flops with low power

consumption "Create fast, low-power sense- amplifier flip-flop Enhance flip-flops' common-mode rejection ratio (CMRR); reduce power consumption during low switching activity; and provide low-power, high-performance sense-amplifier flip- flops. Dealing with flip-flop circuit power consumption and delay reduction using double edge triggered flip-flops in a low power design.

III. EXAMINATION OF PREVIOUS STUDIES

By giving the enabling signals, a full clock cycle to compute and propagate to their gate, it has the significant advantage of evading the strict timing constraints of AGFF and data- driven. Additionally, LACG is independent of the data toggling vectors of FFs, unlike data- driven gating, whose optimization necessitates that knowledge .Regardless of the intended use, the LACG logic embedding in the RTL functional code is specifically defined and readily extracted from the underlying logic. This simplification is beneficial since it makes the gating implementation much simpler [4].

The modeling, analysis, circuits, optimization, and implementation of LACG are covered in the remainder of the work. The pulse generating stage, the sensing stage, and the latching stage are its three stages. DETSAFF both employ the same basic pulse generator. A brief pulse signal that is synchronized at the rising and falling clock edges is produced by the dual edge triggered pulse generator. When a collection of flip- flops are positioned in close proximity to one another, numerous flip-flop circuits can share the pulse generator [4]. SB will be set to high during the evaluation phase of a flip-flop based on a sense amplifier if D is low, and RB will be set to high if D is high. In order to prevent redundant transitions, the conditional pre- charging approach is used in the DET- SAFF sensing step.

IV. PROPOSEDMETHOD

When designing low power circuits, double edge triggered (DET) flip-flops seem like a logical choice because they can retain the same data rate at half the clocking frequency of traditional single edge triggered (SET) flip-flops. This is due to the fact that DET flip-flops need to be charged and discharged half as frequently as SET flip-flops. Unfortunately, the substantial over head in complexity that D ET flip-flops involve has up till now limited their usefulness [3]. Some of the T-effects of a lower clock frequency are counteracted by the DET structures' increased complexity, which denotes higher energy consumption. However, we have created a collection of DET flip-flops that can be constructed by defining a D-type DET flip-flop innermost it’s most basic functional representation. Using Hspice, the suggested architecture is simulated. Conditions in and 90 nm CMOS technology serve as the foundation for this scenario. With a 20 FF capacitor at the Flip- Flop's output and a 3 FF capacitor at the clock buffer's output, as well as an operating state of 1.0 V power supply and 500 MHz CLOCK, the suggested architecture is appropriate for low power applications. Using Hspice, the suggested architecture is simulated .Conditions and 90nm CMOS technology serve as the foundation for this scenario .With a 20FF capacitor at the Flip-Flop's output and a 3 ff capacitor at the clock buffer's output, as well as an operating state of 1.0 V power supply and 500MHz CLOCK ,the suggested architecture is appropriate for low power applications. However, inverters must apply a complemented clock signal in order to use the original MUX2-based FF. A compound OR AND- INVERTER (OAI21) gate and a NAND2 gate topology are used as the MUX2 circuit in order to remove the internal clock inverters for the select(CK) pin using the MUX2 based on OAI21, the MSFF [5].

In the conditional capture technique, clock-gating causes the gate that controls the delivery of the delayed clock to the flip-flop to use redundant power. Therefore, in terms of lowering the flip- flop EDP, the conditional pre-charge strategy outperformed the conditional capture technique .However, only ip-FF has been subjected to the conditional pre- charge technique, and using a double- edge triggering mechanism for these flip- flops is challenging because to the high transistor requirements[6]. This work proposes a novel conditional discharge technique that avoids the issues with the conditional capture technique for both implicit and explicit pulse- triggered flip- flops.

This article describes a wide variety of GNSS LNA topologies, including ones that are linear, stable, have low power in the above range [7]. FN_C-DET catches up as the activity rate is above20%. This means that the lower the switching activity, the more the power dissipation will be saved by adopting the proposed STC-DET topology. This phenomenon is due to the fact that with lower switching activity, there is more

percentage of cycles that the data does not change which increases redundant-transition power in all other DETs. The proposed design shows the best power- delay- product (PDP) performance thanks to its low power and contention- free nature. Note that the area of the STC is large because of the added transistors. But they are used to remove the RTs to achieve significant power saving. For example, it consumes 56% less power than the widely used TGFF [8]. Setup and hold time of FF is important for the design to meet system timing constraints and performance metrics [9]. In this design, the setup time is determined by the propagation delay from *D* to *M I.*

D _n, whereas the hold time is by the speed of *QT* when settling to its final value after the clock transition. The worst case hold time scenario occurs when *D* falls too close to the clock's rising edge, which results in a fall of $M\ I\ D'$; then *Y* in the top slave latch will be pulled up to turn P8 off before *QT* is fully charged to V dd[10].

PROPOSED MODEL:

The pulse generating stage, the sensing stage, and the latching stage are its three stages and DETSAFF both employ the same basic pulse generator. A brief pulse signal that is synchronized at the rising and falling

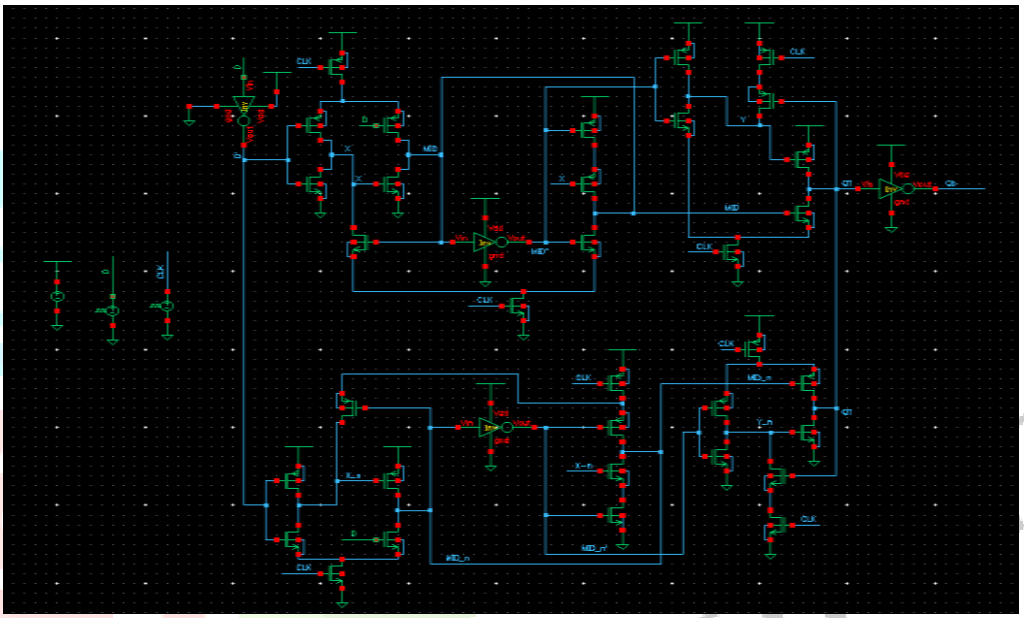

Fig:1:schematicof TSPC

clock edges is produced by the dual edge triggered pulse generator. When a collection of flip-flops are positioned in close proximity to one another, numerous flip-flop circuits can share the pulse generator [11]. SB will be set to high during the evaluation phase of a flip- flop based on a sense amplifier if D is low, and RB will be set to high if D is high. In order to prevent redundant transitions, the conditional pre- charging approach is used in the DET- SAFF sensing step [12].

V. EXPERIMENTAL RESULTS

In this section, we present the experimental results for the redundant-transition-free low power TSPC dual-edge-triggering flip-flop with a clocked single transistor. The performance metrics evaluated include power consumption, propagation delay, and area efficiency.

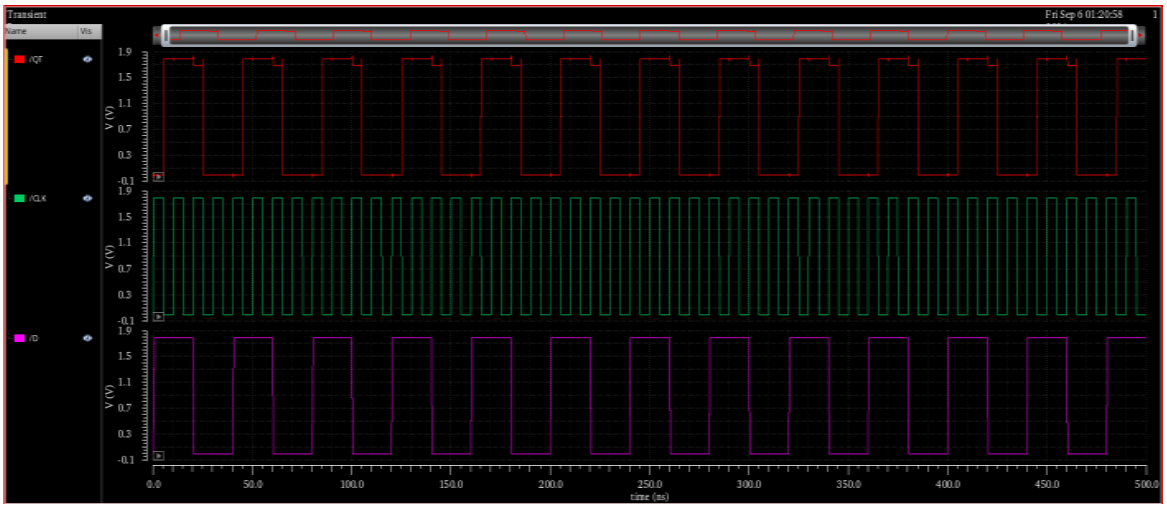

Fig:2:Simulated timing diagram

VI. CONCLUSION

In this work, we presented a redundant-transition-free low power TSPC(True Single-Phase Clock) dual-edge- triggering flip-flop utilizing a clocked single transistor approach. The proposed design effectively reduces dynamic power consumption while maintaining high performance and reliability. By eliminating unnecessary transitions, the flip-flop minimizes power dissipation, making it suitable for power-sensitive applications.

The dual-edge triggering mechanism enhances the overall throughput, allowing for more efficient data processing without increasing clock frequency. Simulation results confirm that our design outperforms conventional flip-flops in terms of power efficiency and speed, while also demonstrating robustness against variations in temperature and supply voltage.

Future work may explore the integration of this flip- flop in larger circuits and its performance in various operating conditions, further validating its effectiveness in low-power digital designs. Overall, the proposed flip- flop represents a significant advancement in the development of energy-efficient digital systems.

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