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Development Of High Performance Standard Cell Library In Sub-Micron Technology For High Speed Applications – A Review

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Abstract

The recent usage of deep sub-micron tenure was due to the rise in demand for integration of much more components on to a single chip for better performance with less power consumption. ASIC consists of logic blocks which are pre-designed and pre-verified in system library functions which lead to the success for the rapid increase of integrated system. Standard cell methodology is a phenomenon of designing ASICs (Application Specific Integrated Circuits) that is used in designing semiconductors with digital-logic features [1]. The cells or logic gates selected to build the library depends on the design requirement. These cells when used in the Semi-Custom Design Flow have to meet certain functions and performance. A successful and efficient implementation of a Semi-Custom Design depends on the standard cells in the library. Therefore, it is important to have a high quality cell library [2]. Modern integrated circuits are very large containing over a billion of transistors. Designs based on sub-micron technologies will always be a challenging task for the manufacturer to produce it at a very competitive cost. One approach is to use 'Cell-Based' implementation using Standard cell library [3]. Standard cells allow tools to automatically

synthesize a circuit and optimize area, power consumption and timing. The state of the art Standard Cell Library using CMOS technology

In this paper, overview of survey on history and development of standard cell library by considering different specifications like area, power, speed and driving strength in different technology(90nm, 65nm, 45nm and so on) for different applications is discussed.

Keywords: AutoCelllib, CADENCE, CMOS, DSM technology, FinFet, Standard Cell Library, Low Power

1. Introduction

VLSI Design answers not only the question of "What is VLSI", but also shows how to use VLSI. A general VLSI design flow is shown in **Figure1** below. Design start at the behavioral level and then proceed at structural level. In this, the design is partitioned into the front end stage at the behavioral level and the back end at the structural and physical level. This is important because it illustrates a partitioning that is used to build Application Specific Integrated Circuits (ASICs). In an ASIC, the design can be developed at the HDL (hardware description language) level and then passed to a company that completes the transition from to an actual chip. In this way, the original design company does not have to invest the personnel or tools required to translate in HDL specification into a physical chip.

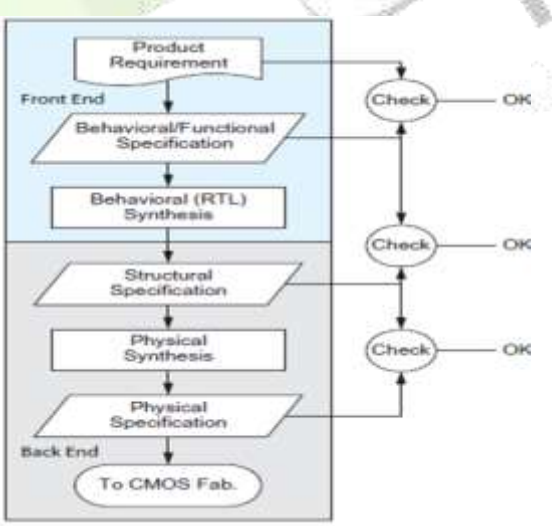

Figure 1: VLSI Design Flow [4]

A chip designed to perform a specific operation rather than a general purpose chip such as a microprocessor. The use of ASICs improve the performance over general-purpose CPUs, because ASICs are hardwired to do a specific job and do not incur the overhead of fetching and interpreting the stored instructions.

Types of ASICs: The classification of ASICs is shown in the figure 2 below. It is broadly classified into three types [5].

1. Full Custom ASICs
2. Semi-custom ASICs
3. Programmable ASICs

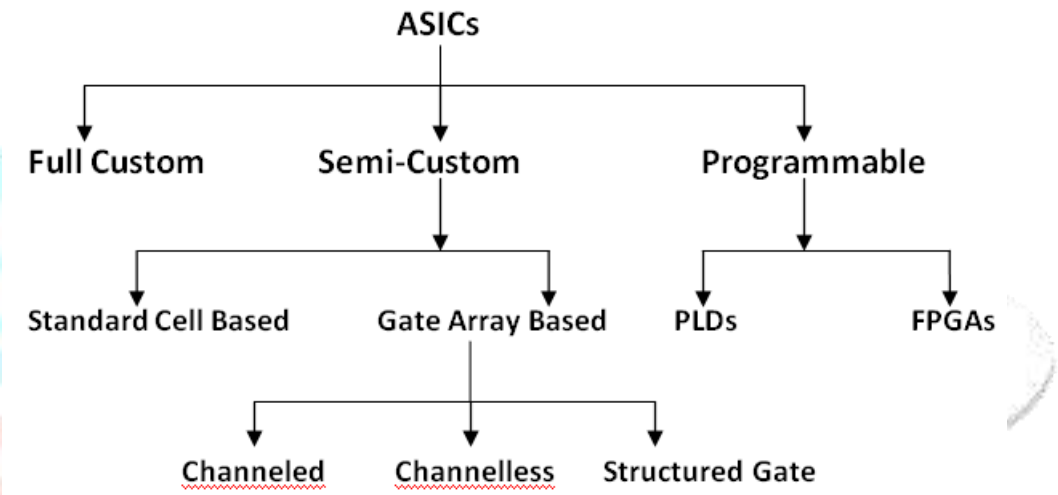

Figure 2: Classification of ASICs [5]

1. Full Custom ASICs: A Full custom ASIC is one which includes some (possibly all) logic cells that are customized and all mask layers that are customized. A microprocessor is an example of a full-custom IC. Designers spend many hours squeezing the most out of every last square micron of microprocessor chip space by hand. Customizing all of the IC features in this way allows designers to include analog circuits, optimized memory cells, or mechanical structures on an IC, for example. Full-custom ICs are the most expensive to manufacture and to design. In a full-custom ASIC an engineer designs some or all of the logic cells, circuits, or layout specifically for one ASIC. This means the designer avoids using pretested and pre characterized cells for all or part of that design. One has to use full-custom design if the ASIC technology is new or so specialized that there are no existing cell libraries or because the ASIC is so specialized that some circuits must be custom designed. The growing member of this family, now a days is the mixed analog/digital ASIC.

2. Semi-Custom ASICs: ASICs, for which all of the logic cells are predesigned and some (possibly all) of the mask layers are customized are called semi custom ASICs. Using the predesigned cells from a cell library makes the design, much easier. There are two types of semicustom ASICs (i) Standard-cell–based ASICs (ii) Gate-array–based ASICs. A cell-based ASIC (cell-based IC, or CBIC pronounced sea-bick) uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops, for example) known as standard cells. The advantage of CBICs is that designers save time, money, and reduce risk by using a predesigned, pretested, and pre characterized standard-cell library. In addition each standard cell can be optimized individually. During the design of the cell library each and every transistor in every standard cell can be chosen to maximize speed or minimize area. The disadvantages are the time or expense of designing or buying the standard-cell library and the time needed to fabricate all layers of the ASIC for each new design.
3. Programmable ASICs: Programmable logic devices (PLDs) are standard ICs that are available in standard configurations. However, PLDs may be configured or programmed to create a part customized to a specific application, and so they also belong to the family of ASICs. PLDs use different technologies to allow programming of the device. The simplest type of programmable IC is a read-only memory (ROM). The most common types of ROM use a metal fuse that can be blown permanently (a programmable ROM or PROM). An electrically programmable ROM, or EPROM, uses programmable MOS transistors whose characteristics are altered by applying a high voltage. There is another type of ROM that can be placed on any ASIC a mask-programmable ROM (mask-programmed ROM or masked ROM). A masked ROM is a regular array of transistors permanently programmed using custom mask patterns. So, an embedded masked ROM is a large, specialized, logic cell.

Field-Programmable Gate Arrays (FPGAs) are the newest member of the ASIC family and are rapidly growing in, replacing TTL in microelectronic systems. There is very little difference between an FPGA and a PLD .An FPGA is usually just larger and more complex than a PLD. In fact, some vendors that manufacture programmable ASICs call their products as FPGAs and some call them as complex PLDs [5].

1.1. Standard Cell based ASICs

A cell-based ASIC (cell-based IC, or CBIC pronounced sea-bick) uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops, for example) known as standard cells. The advantage of CBICs is that designers save time, money, and reduce risk by using a predesigned, pretested, and pre characterized standard-cell library. In addition each standard cell can be optimized individually. During the design of the cell library each and every transistor in every standard cell can be chosen to maximize speed or minimize area. The disadvantages are the time or expense of designing or buying the standard-cell library and the time needed to fabricate all layers of the ASIC for each new design.

The increasing demand for system integration by combination of transistors along with less power dissipation has been in development with the CMOS technology. The recent usage of deep sub-micron tenure was due to the rise in demand for integration of much more components on to a single chip for better performance with less power consumption. ASIC consists of logic blocks which are pre-designed and pre-verified in system library functions which lead to the success for the rapid increase of integrated system. This further helped designers to reduce the time for product development and to manage ramifications by adding more and more transistors. Standard cell methodology is a phenomenon of designing ASICs (Application Specific Integrated Circuits) that is used in designing semiconductors with digital-logic features. It is shown as an example of design consideration by enclosing the low-level VLSI- layout into an abstract logic representation [1].

1.1.1 Standard Cells Library: Standard cell library is an integral part of ASIC design flow and it helps to reduce the design time drastically. Standard cell library is a collection of well defined and pre-characterized logic cells with multi-drive strength and multi-threshold voltage cells in the form of a predefined standard cell layout. It also contains a number of physical only cells and a set of library files required by Place and Route (PnR) tool for automatic placement and routing (APR). A standard cell used in the ASIC design is a part of a standard cell library along with some other file sets.

Cell Collections:

In general, a standard cell library contains the following types of cell [6]:

- All basic and universal gates (like AND, OR, NOT, NAND, NOR, XOR etc)
- Complex gates (like MUX, HA, FA, Comparators, AOI, OAI etc)
- Clock tree cells (like Clock buffers, clock inverters, ICG cells etc)
- Flip flops and latches
- Multi-drive strength cells
- Multi-Vt cells
- Physical only cells
- Scannable Flip flops

Multi-drive strength cells:

A low drive strength cell will require less power and area but having more delay and more transition time whereas a high drive strength cell can drive a larger number of cells and having a fast transition. So as per the requirement, a PnR design engineer chooses the drive strength of cells to optimize the area, power and performance.

Multi-V_T cells:

A low threshold voltage (LV_T) cell will have a lesser delay but higher leakage power as compared to a high threshold voltage (HV_T) cell. So, as per the requirement of timing and power a PnR engineer uses HV_T and LV_T cell to balance the power and timing of the design. There is no difference in the area on multi-Vt cells. A modern standard cell library contains generally ULV_T, LV_T, SV_T, HV_T types of cells in which V_T is in increasing order.

Physical only cells:

In physical design, we need to add a variety to standard cells to mitigate various effects and manufacturing issues. These cells do not have any logical functions. For example to overcome the latch-up issue we need to add well tap cells. Decap cells, endcap cells, antenna cells and filler cells are the example of such cells.

File Collections:

Apart from the standard cells, Standard cell library is delivered with a collection of files which contains all the information required to auto place and route. These files are mainly:

- **LIB files (.lib)**
- **LEF files (.lef)**
- **Netlist file (.v)**
- **GDS file (.gds)**
- **SPICE Netlist (.sp)**
- **Model file (.m)**

All the format of files mentioned here with the reference of the Cadence tool. Some files format is different in the Synopsys tool but the information inside the file is the same. Brief information of these files is given below.

Timing library (LIB or DB) files are generated during the characterization of cells. Library files contain cell delay, power and area information. Physical library (LEF) file is an abstract view of the layout of the cells. LEF file contains the information of cell boundary, Pins inside the cell, location, direction, and metal layer of each pin. Netlist file is a Verilog file of the standard cell which defines the functionality of a cell. GDS file is the layout of the standard cell. SPICE netlist is the netlist of cell in SPICE format is used for simulation. Model file contains the various design parameters of the cell required for SPICE simulation.

1.1.2 Choice of Standard Cells Library:

Standard cell library contains a collection of components that are standardized at the logic or functional level, and consists of cells or macro-cells based on the unique layout. SCLs are used for a large range of applications. The use of a SCL drastically reduces the cost of designing a chip. It also reduces the time-to-market, which results in lower production cost, early sales, longer time in marked, etc. The economic and efficient accomplishment of an IC design depends heavily upon the choice of the library. Hence it is important to build library that full fills the design requirement [7, 1].

A technology library is formed by a complete group of standard cell descriptions. The choice of library decides the efficiency and economic accomplishment of ASIC design. Digital standard cells are used in a variety of integrated systems. These systems have a wide variation in design requirements. In some

systems, power consumption is critical, in others minimal silicon area is driven by cost, and in some systems operating speed is the dominant consideration. Given the varying requirements of system designs and the widespread usage of digital standard cells, it is desirable to have standard cell libraries which are tuned to these specific needs.

1.1.3 ***Types of Standard Cell Library:***

Standard-cell library offering is usually divided according to the 1) Density and 2) Threshold Voltage (V_{TH}).

Classification according to the Density: It is illustrated in the figure3 given below.

- Ultra High Density(UHD)- 7 Track or 8 Track Library for cost driven requirements
- High Density(HD)- 9 Track/10 Track Library for main stream requirements
- High Performance (HP) – 12 Track Library for high-speed requirements

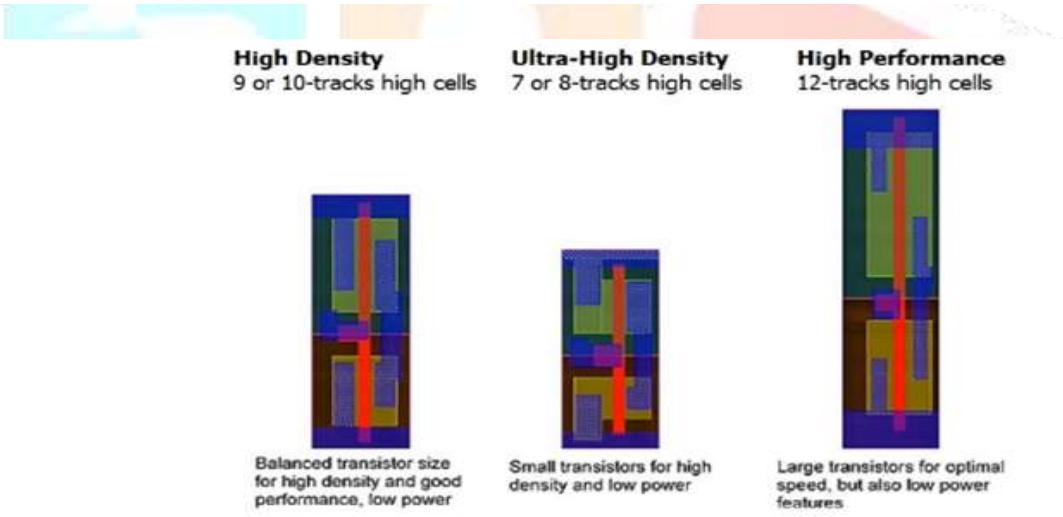

Figure3: Classification according to the density

Classification according to the Threshold Voltage (VTH):

- Low VT(LVT) – Fast because of low Gate Delay, but high leakage
- Standard VT(SVT) or Regulr VT (RVT)
- High VT (HVT) - Low Leakage, but slow because of High Gate Delay
- Metal 2 pitch is used to calculate the Number of Tracks in different Density Libraries
- Sub-threshold Leakage varies exponentially with VTH compared to the weaker dependency of Delay over VTH
- HVT Cells are used in Non-critical paths to meet Timing

Comparative analysis between three types of standard-cell libraries:

Three types of standard cell library for implementing logic of the always-on power domain are considered for the comparison as shown in the Table1.

Table1: Comparison of three types of Standard Cell Library [5]

Library type	Description
Conventional high-density standard-cell library	Typically based on 6 or 7 tracks, optimized for high-density, using HVT devices (if this layer is available) and supplied at nominal voltage. Reference in Dolphin integration catalog: SESAME HD & SESAME uHD
Standard-cell library optimized to operate down to ultra-low voltage	Library specifically designed with core transistors to operate safely Near Threshold Voltage with a reasonable speed degradation to support speed requirements of an Always-on logic. Reference in Dolphin integration catalog: SESAME NTV
Standard-cell library supporting extended operating voltage range	Implemented with thick-gate-oxide transistors, the advantage is twofold: an extended voltage range enables a direct connection to the battery (if not higher than 3.6 V), thus avoiding the need for any voltage regulator, and thick gate-oxide transistors leak significantly less than core transistors. Reference in Dolphin integration catalog: SESAME BIV

1.1.4 Challenges associated with the designing of standard cell libraries

We observe that the key challenges limiting the quality of the standard cell library are:

Challenge #1**:** *Pin accessibility in standard cell*

As the standard cell layouts are drawn with minimum design rules to maximize the benefit of design area shrinkage, the number of routing tracks has begun to decrease from 12-track in 65-nm to 7.5-track in 14-nm. As a result, the modern router tools have difficulties with signal routes accessing to the standard cell pins. In particular, the challenges with pin-access have severely degraded routing resource estimation accuracy with the convention global and detail routing model. Multiple design iterations are required to resolve the routing congestion and pin accessibility issues, or even required in a change in the design core utilization, thus resulting in an increase in the overall chip area [8].

Challenge #2**:** *Power, Ground and Clock Need Wider Wires*

The power supply needs to be distributed to all the cells in the circuit. Resistance in these lines must be very small, since when a gate switches current flows through the supply lines. If the resistance of the supply lines is too large, the voltage supplied to gates will drop, which can cause the gate to malfunction.

Challeng #3: *Electromigration*

Electromigration is the phenomenon of metal atoms physically moving over time (months). Wires and contacts can thin out and break. It occurs both in signal (AC=Alternating Current direction) and power wires (DC = Uniform Current direction). But problem is 10 times more severe for the same current if DC rather than AC. The DC currents occur in two places: Inside of cells, and in the power busses. So,

sometimes need more contacts on transistor sources and drains to meet electromigration limits. And width of power buses must support both iR and electromigration requirements [9].

Challenge #4*: Signal Integrity issues in DSM technologies*

Crosstalk delays and crosstalk coupling noise are the preliminary signal integrity effects that occur in DSM technologies due to shrinking feature sizes, increased resistive and capacitive values of on chip routing, leading to increased delay unpredictability, which can be a potential source of malfunction of a SOC.

Capacitive crosstalk can induce noise (glitches) on a non-switching signal line routed with a switchable signal line, and can potentially cause functionality failures. Similarly, crosstalk can cause increased delays when an aggressor switches in the opposite direction of the victim. Conversely, an aggressor can cause decreased delays when switching in the same direction as the victim. This increase or decrease in delays can cause setup or hold time violations respectively, and may lead to reduced operating frequency and functional failures [10].

Challenge #5*: Reliability issues*

Even though transistor dimensions scale according to the ITRS roadmap [3], it is doubtful whether Moore's law will be valid for the sub-45nm nodes. Performance gains are likely to saturate, despite the continuous shrinking of channel length. Gate leakage will dramatically rise from the 45nm node on. Process variability-induced effects and progressive reliability wear-outs like NBTI in PMOS transistors will pose significant threats for the lifetime of modern Systems-on-Chip (SoCs) [11].

These effects have a negative impact on the development of industrial design kits and transistor-level models for technologies below 45nm, which is now the state-of-the-art.

2. Problem Statement

- As the complexity of design continue to increase, full custom is no longer feasible. Designs based on different technology at competitive cost have always been challenges to manufacturers.
- Some of the driving factors including portability, mobility, accuracy and increased performance demands.
- This brings the manufacturers to adapt certain methods such as decrease component sizes, increase its performance simultaneously, and improve heat tolerance materials and so on.
- To design every logic gate at different driver strength will be more time consuming.

- These factors motivate to go semi-custom design for creating own Standard Cell Library with specified specifications at different driving strength in sub-micron technology for a large range of applications.

3. Literature Survey

Custom standard cell libraries can improve the final quality of the corresponding VLSI designs but properly customizing standard cell libraries remains challenging due to the complex characteristics of the VLSI designs. According to the post-technology mapping gate-level netlist of the design and the initial standard cell library, AutoCellLibX can find a set of standard cell cluster pattern candidates that occur frequently based on our proposed high efficiency sub-graph mining algorithm for gate-level netlist. AutoCellLibX closes the optimization loop between the analysis of gate-level netlist and standard cell library customization for VLSI design productivity. The experiments with FreePDK45 library and benchmarks from various domains show that AutoCellLibX can generate the library extension with up to 5 custom standard cells in 1184 seconds on average for the benchmarks and the resultant extension of the standard cell library can save design area by 4.49% averagely [27].

As devices are becoming smaller, slimmer, faster, and more efficient, the transistors also have to keep up with the demands and needs of the daily user. Unfortunately, the CMOS technology has reached its limit and cannot be used to scale down due to the transistor's breakdown caused by short channel effects. An alternative solution to this is the FinFET transistor technology, where the gate of the transistor is a three dimensional fin that surrounds the transistor and prevents the breakdown caused by scaling and short channel effects. In this work, the FinFET package file used to design standard cells in a 15nm FinFET technology file developed by Cadence and Mentor Graphics [28].

Analog and mixed-signal standard cells enable compilation of a high-level description of analog and mixed signal designs to full IC layout. A standard cell library definition allows components designed in any process to have broad utilization. A high-level to layout compilation empowers rapid movement between different IC processes. In this work, a mixed-signal cell library built through multiple generations of educational experiences. Digital standard cell libraries are ubiquitous for commercial and academic IC design. Analog standard cell libraries are rare within system-level analog design. Educational efforts in analog system design provide a path for developing these standard cell libraries [29].

The advancement in the Internet of Things (IoT) field is widely notified. The number of IoT applications seen in daily life is increasing in significant engineering fields. In this work, a CMOS Standard Cell Library of low-energy, minimum-area, and fitted for IoT applications is introduced. This paper uses two solutions to provide significant energy saving. The UMC 130nm CMOS process technology was used to design and characterize the proposed library. The maximum achieved frequencies are 14MHz, 18MHz, and 16MHz, and the corresponding energy consumption is 4.25 pJ, 10.03 pJ, and 30.57 pJ, respectively [30].

Sangmesh Melinmani et.al developed 1.8V high density 9 track Standard Cell Library in 180nm technology with operating -40^{o}C to 125^{o}C temperature. In this design, 144 cells have been designed which include logical cells, sequential cells and special cells. Each cell has the following views: schematic, symbol, layout and abstract. Once a cell is fully verified, an abstract view can be generated. Cadence Abstract generator is used to generate the physical description i.e., the abstract view and the Layout Exchange Format (LEF) file for all the cells. Each standard cell has its electrical characterization for three different process corners, for a range of input slew and output load [3].

Designing standard cell layouts with fixed height as well as maintain a standard cell template based design for all the standard cells in the given library. So automatically reduce the area of the standard cells and one more objective is characterizing the standard cell using Liberate. The Future work involves developing UDPs (User Development Programs) for all standard cells. That means to generate Verilog and VHDL functional simulations [12].

Designs based on different technology at competitive cost have always been challenges to manufacturers. The economic and efficient accomplishment of an IC design depends heavily upon the choice of the library. Therefore, it is important to build library that fulfils the design requirement. One way to understand the required layout characteristics of standard cells is to understand their history and the reasons behind their development. The Cells or logic gates selected to build the library depends on the design requirement. These cells when used in the Semi-Custom Design Flow have to meet certain functions and performance. In this library Software used to design is cadence software .The cells are either area optimized or speed optimized. The area optimized cells uses minimum sized transistors while the speed optimized cells uses larger transistors to provide good driving capabilities. In this work high performance standard cell library is

designed for the supply voltage of 1.8V, number of tracks used are 12, Cell Height of 8.64um, operating with temperature range of -40 oC to +125 oC [13].

With the increasing number of transistors in a single integrated circuit, power is becoming one of the major issues in integrated circuit development. This issue requires additional effort from designers in order to produce lower power standard cell designs. The purpose of this work is to develop a standard cell library using Taiwan Semiconductor Manufacturing Company's 0.18-micron CMOS technology. TGMOS is also a logic style which requires improvements. Speed is becoming the issues for TGMOS. Future works may include combining domino based logic with transmission gate logic style in order to achieve low power and higher speed compared to standard CMOS logic [14].

With demand for more and more system on chip, the complexity of the (IC) fabrication had also increased as complex layout issue had to be taken in to consideration. A 3.3V Digital standard Cell Library has been developed for LEON3 operable at 200°C temperature. For the library, SOI process is used as it has some advantage over the bulk. Future work includes, in the library, some more cells can be added as a combination of AO (ANDOR) and AOI (ANDOR INVERTED) [15].

The use of sub-threshold digital circuits is ideal in some scenarios to achieve optimized power/speed tradeoffs. This paper discusses the design of a sub-threshold standard cell library using a standard 0.18-Pm CMOS technology. A complete library of 56 standard cells is designed and the methodology is ensured through schematic design, transistor width scaling and layout design, as well as timing, power and functionality characterization with a nominal supply voltage of 1.8V and the threshold voltages are Vtn = 0.482V and Vtp = 0.462V [16].

In highly-scaled CMOS technologies, analog and digital functionality are often combined into more powerful systems. Design of a custom digital library becomes a necessary step for a successful mixed-signal design. In this paper, the design of such a custom digital library is presented. The library was designed in 28nm CMOS technology with 14- track footprint and tailored for usage in mixed-signal applications. Finally, the performance of the library is compared to two other digital libraries, one of which is a state-of-the-art commercial library based on high performance 45nm silicon-on-insulator (SOI) CMOS technology. The designed library offers low leakage power and low area consumption while allowing moderate speed which is well suited for the usage in digital control blocks within the mixed-signal systems [22].

Libraries for ultra-low voltages need to be fully redesigned according to criteria that are very different from traditional above threshold libraries. In sub-threshold CMOS circuits, the consumption is reduced by aggressively reducing the operating voltage V_{DD}, which is lower bounded by the minimum value $V_{DD,min}$ that ensures correct operation. Below $V_{DD,min}$ CMOS logic gates are not capable to correctly switch. Since the system-level minimum voltage is dictated by the cell having the largest $V_{DD,min}$, sub-threshold standard cell libraries need to be designed to minimize the maximum $V_{DD,min}$ across all cells [17].

Processor operating over a wide voltage range achieves better possible energy efficiency while satisfying varying performance demands of the applications. In order to meet that efficiently, a standard cell library specific for wide voltage operation is necessary. In this work, a 40nm 0.3V-1.1V CMOS standard cell library by using sizing method to optimize the original one provided by foundry [18].

Table 2 shows the comparison of development of Standard Cell Library in different technology process in detail.

Table 2: Comparison of development of Standard Cell Library in different technology

Author Name	Year	Title	Software tool used	Specifications	Research Gap
Tingyuan Liang et.al	2022	AutoCellLibX: Automated Standard Cell Library Extension Based on Pattern Mining	AutoCell LibX	FreePDK45 library and benchmarks from various domains show that AutoCellLibX can generate the library extension with up to 5 custom standard cells within 1.1 hours for each of the 31 benchmark designs and the resultant extension of the standard cell library can save design area by 4.49% averagely.	AutoCellLibX closes the optimization loop between the analysis of gate-level netlist and standard cell library customization for VLSI design productivity.
Phanindra Datta Sadhu	2021	Design and Characterization of Standard	CADENCE	A standard cell library was designed and	Foundries and designers in the industry have

		Cell Library Using Finfets		implemented using FinFETs using 15nm.	started implementing designs sub 5nm node sizes and are looking to scale them further down to improve the performance of their designs.
AbdelRahaman Hesham	2021	Design and Implementation of energy efficient near-threshold standard cell library for IoT applications.	CADENCE	UMC 130nm CMOS process technology. Frequency Range: 1-20 MHz	A CMOS Standard Cell Library of low-energy, minimum-area, and fitted for IoT applications is introduced. Two methods are used to design the library. One will be operating in the near threshold region and the second is to create layouts at the minimum possible area.
Jennifer Hasler et.al	2020	Defining Analog Standard Cell Libraries for Mixed-Signal Computing enabled through Educational Directions	CADENCE		A mixed-signal cell library built through multiple generations of educational experiences. Digital standard cell libraries are ubiquitous for commercial and academic IC design. Analog standard cell libraries are rare within system-level analog design. Educational efforts in analog system design provide a path for developing these standard cell libraries.
Author Name	**Year**	**Title**	**Software Tool Used**	**Specifications**	**Research Gap**
Sangmesh Melinmani	2019	Standard Cell Library Development	CADENCE	Developed1.8V high density 9 track Standard Cell Library in	For each standard cell, physical characteristics are given in a LEF file,

				180nm technology with operating -40°C to 125°C temperature	which is used in the automation of the design of standard cell based ICs and is widely accepted among CAD tools.
Naga Lavanya M et.al	2018	Design and Development of an ASIC Standard Cell Library Using 90nm Technology Node	CADENCE	90 nm technology, No. Of Tracks: 15, No. Of Cells used: 200.	Future work involves developing UDPs (User Development Programs) for all standard cells.
Jan Pliva et.al	2017	Design of a Custom Standard-Cell Library for Mixed-Signal Applications in 28 nm CMOS	CADENCE	A full custom standard cell library was designed in 28 nm CMOS. The library was used for a synthesis and fabrication of a 32 byte SPI.	The designed library is well suited for the intended design of configuration interfaces in mixed-signal circuits
Somayeh Timarchi	2016	Ultra-Low Voltage Standard Cell Libraries: Design Strategies and a Case Study	CADENCE	A standard cell library is designed in 180-nm CMOS technology	Guidelines to design standard cell libraries for sub-threshold operation have been derived and discussed
Jintao Li1	2015	0.3V-to-1.1V Standard Cell Library in 40nm CMOS	CADENCE	40nm 0.3V-1.1V CMOS standard cell library. 4.5%-6.9% speed improvement and 6.7%-22.3% less power comsumption synthesized at 0.6V compared with the foundry-provided one.	By using sizing method to optimize the original one provided by foundry. Better noise margin under process variation at 0.3V and 0.6V, faster speed at 0.6V and 1.1V

Prof. Poornima H S et.al	2014	Standard Cell Library Design and Characterization using 45nm technology	CADENCE	45nm CMOS process	In future more investigations have to be done on the behavior of transistors in series. To improve the efficiency of the library for building complex design, mega cells such as: 1 bit register file slice, a 1 bit ALU, p-decoder, UART, PIO/PIA microcontroller core, fixed point DSP core, FIFO, SRAM should be included in the existing library.
Author Name	**Year**	**Title**	**Software tool used**	**Specifications**	**Research Gap**
Mr. Narhari R. Kotkar M.E.	2014	Development Of High Performance Standard Cell Library In Umc180nm Technology	CADENCE	Supply Voltage -1.8V, Operating Frequency -500MHz , Number of tracks-12, Cell Height - 8.64um Temperature Range	The cells are either area optimized or speed optimized. The area optimized cells uses minimum sized transistors while the speed optimized cells uses larger transistors to provide good driving capabilities.
Ming-Zhong Li et.al	2013	Sub-threshold Standard Cell Library Design for Ultra-Low Power Biomedical Applications	CADENCE	56 standard cells based on a standard 0.18-µm CMOS technology are created under an identical power supply voltage of 0.3V to 0.45V. The sub-threshold library based FIR	The major drawback is the increase in the number of cells of about 1. 76 times, resulting in an increase in area. Further study is under-going for the optimization of the SCL.

				filter design achieves a power savings of 95.62% and a leakage power reduction of 97.54% comparing with the same design implemented by the commercial SCL.	
REHAN AHMED	2009	Design Of 3.3v Digital Standard Cells Libraries For Leon3	CADENCE	A 3.3V Digital standard Cell Library has been developed for LEON3 operable at 200°C temperature.	For the library, the SOI process is used as it has some advantage over the bulk.
Suryadi Gunawan	2003	0.18µm CMOS low power standard cell library	Mentor Graphic tools	Successfully developed a 0.18 micron CMOS Low Power Standard Cell Library containing 34 cells.	Future works may include combining domino based logic with transmission gate logic style in order to achieve low power and higher speed compared to standard CMOS logic.

4. Objective of the Proposed Research:

Growing demand for microelectronics in several applications has been directly impacting the growth of programmable application specific integrated circuit (ASIC) market. With the advent of smart devices, electronic products such as smartphones, tablets, laptops and other mobile devices have witnessed immense penetration across the world. Additionally, due to consistently growing adoption of mechatronics across the automotive and industrial applications, the demand for related electronic components (such as ASIC) has witnessed dramatic growth over the period of time as sketched in figure 4. Growing use of application integrated circuits in the IT & telecommunication is a driving factor for the programmable application specific integrated circuit (ASIC) market.

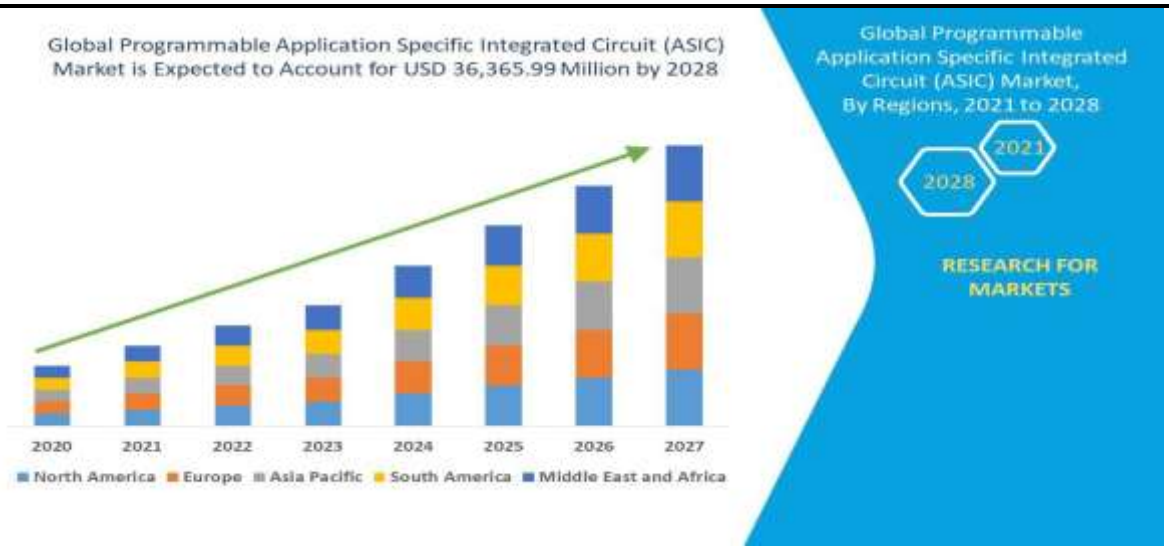

Figure4: Expected graph of Global Programmable ASIC Market [19].

High cost of producing and manufacturing customised circuit is a challenge for the programmable application specific integrated circuit (ASIC) market. However, inflexibility and increased time-to-market is the main restraint for the growth of programmable application specific integrated circuit (ASIC) market during the forecast period of 2021- 2028. Hence, it is necessary to design and develop high performance standard cell library consisting of basic and universal gates, Combinational and sequential circuits with different driving strength in sub-micron technology for high speed applications.

5. Methodology:

Cell-based methodology-the general class to which standard cells belongs — makes it possible for one designer to focus on the high-level (logical function) aspect of digital design, while another designer focuses on the implementation (physical) aspect. Along with semiconductor manufacturing advances, standard cell methodology has helped designers scale ASICs from comparatively simple single-function ICs (of several thousand gates), to complex multi-million gate system-on-a-chip (SoC) devices.

The Design flow of SCL is mainly divided into Front end and Back end processes. In Front end design, the following processes will be done:

"Front end" Design:

- System specification and architecture
- HDL (verilog or VHDL) coding
- Behavioral Simulations using RTL(HDL)
- Synthesis

- Gate-level simulations

"Back end" Design:

- Floorplanning, Power grid design
- Standard-cell Placement
- Interconnect routing
- DRC (Design Rule Check)
- LVS (Layout vs Schematic)
- Dynamic simulation and static timing analysis

Design flow of SCL consists in designing a set of logical gates, combinational and sequential circuits for a given technology process. Overview of steps required to design SCL are depicted in the figure5 as shown below.

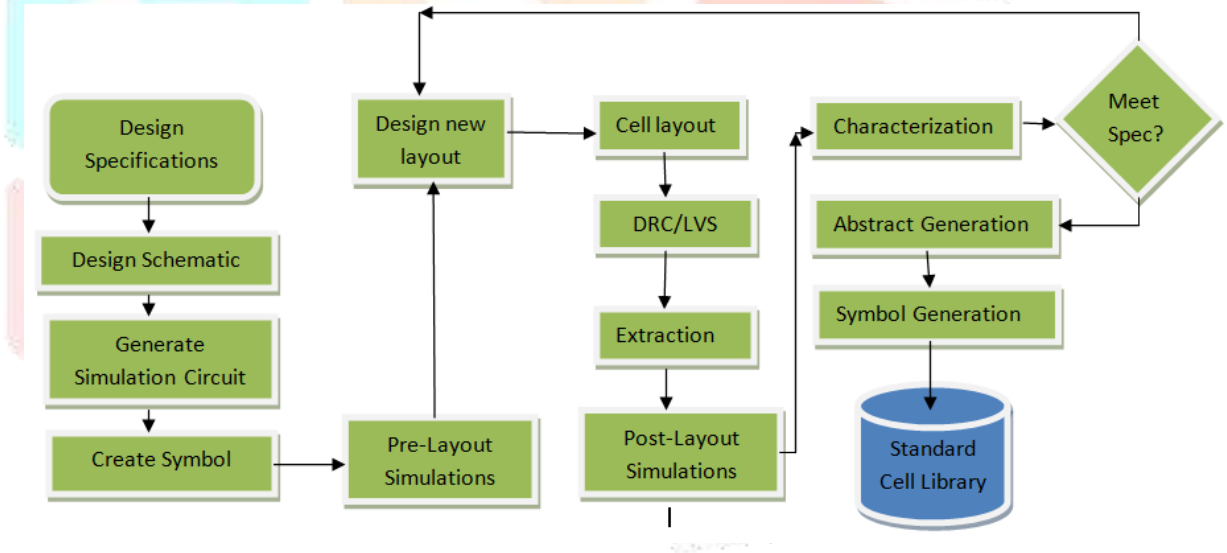

Figure 5: Design Flow of a Standard Cell Library

Steps used in the methodology of Standard Cell Library are explained as follows [20].

Step1: Design Specifications

The specifications typically describe the expected functionality of the designed circuit as well as other properties like delay times, area, etc. To meet the various design specifications certain design trade-offs such as area v/s speed are required.

Step 2: Schematic Design

A Schematic Editor is used for capturing (i.e. describing) the transistor-level design. The Schematic Editors provide simple, intuitive means to draw, to place and to connect individual components that make up the

design. The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections. From the schematic, a netlist is generated, which is used in later stages of the design.

Step 3: Symbol Creation

The schematic capture of the circuit topology is usually followed by the creation of a symbol to represent the entire circuit. The symbol creation will also help the circuit designer to create a system level design consisting of multiple hierarchy level.

Step 4: Pre-Layout simulation

After the transistor level description of a circuit is completed using the schematic editor, the electrical performance and the functionality of the circuit must be verified using a simulation tool. Based on simulation results, the designer usually modifies some of the device properties in order to optimize the performance.

Step 5: Layout

The creation of the mask layout is one of the most important steps in the full-custom design flow, where the designer describes the detailed geometrics and the relative positioning of each mask layer to be used in actual fabrication, using a Layout Editor. Physical layout design is very tightly linked to overall circuit performance since the physical structures determines the transconductances of the transistors, the parasitic capacitances and resistances, and obviously the silicon area which is used to realize a certain function. But the process is very intensive and time-consuming design effort. It is also extremely important that the layout design must not violate any of the layout design rules, in order to ensure a defect free fabrication of the design.

Step 6: Design Rule Check (DRC)

The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built in to the layout editor called Design Rule Checker, is used to detect any design rule violations during and after the mask layout design. If errors are detected, they should be removed from the mask layout, before the final design is saved.

Step 7: Circuit Extraction

After the mask layout has been made free from design rule errors, circuit extraction is performed to create a detailed netlist for the simulation of the circuit. The circuit extractor identifies the individual transistors and

their connections as well as the parasitic capacitances and resistances that are inevitably present. The extracted netlist can give a very accurate estimation of the device dimensions and device parasitics that ultimately determine the circuit performance. The extracted netlist are used in transistor level simulations and in Layout Verses Schematic comparison.

Step 8: Layout VS Schematic Check

After the mask layout design of the circuit is completed, the design should be checked against the schematic circuit description created earlier. The „Layout Verses Schematic (LVS) Check" will compare the original network with the one extracted from the mask layout. The LVS step provides an additional level of confidence for the integrity of the design, and ensures that the mask layout is a correct realization of the intended circuit topology. If any errors show up during LVS, then it should be corrected before proceeding to post layout simulation.

Step 9: Post-Layout Simulation

The electrical performance of a full custom design can be best analyzed by performing a post-layout simulation on the extracted circuit netlist. The detailed simulation performed using the extracted netlist will provide a clear assessment of the circuit speed and the influence of circuit parasitics. If the results of the post-layout simulation are not satisfactory, the designer should modify the transistor dimensions or the circuit topology, in order to achieve the desired circuit performance. Thus, it may require multiple iterations on the design, until the postlayout simulation results satisfy the original design requirements.

Step 10: Characterization

Before including a standard cell into standard cell library, the cells are gone through schematic design, simulations followed by Symbol creation, layout design (as per standard cells layout rules), physical verifications, abstraction, extraction and characterization. So the cells available in standard cell library are free from any DRC violations, well-characterized and suitable for PnR tool for automatic placement and routing.

Library Exchange Format (LEF): The Physical Library or Library exchange format is an ASCII data format, used to describe a standard cell library. It includes the design rules for routing and the abstract of the cells. A LEF file contains the following sections:

- Technology: This file contains all the details about the metal layer information, design rules, via definitions, metal capacitance etc.

- Site: Site extension Info.
- Macros: cell descriptions, cell dimensions, layout of pins and blockages, capacitances.

The technology is described by the Layer and via statements. To each layer the following attributes may be associated [21]:

- Type: Layer type can be routing, cut (contact), masterslice (poly, active), overlap.
- Width/Pitch/Spacing rules
- Direction
- Resistance and Capacitance per unit square
- Antenna Factor

6. Conclusion:

As the technology grows in a faster rate with high expectation, it is required to design the optimized Standard Cell Library which works more efficiently with high performance for different applications. Therefore, in this paper, a detailed survey of designing Standard Cell Library in different technology (180nm, 90nm, 45nm, 40nm and 28nm) by considering different logical and electrical parameters have been discussed. With reference to this survey, further improvements in the design and development of the Standard Cell Library will be performed for real time high speed applications.

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