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A Novel Design of Low-Power High-Speed Double Tail Dynamic Latch Comparator with SAPON Tail Latch

Satish Yadav[1], Pallavee Jaiswal[2]

[1]*Student, Department of Electronics and Communication Engineering, Dr. C. V. Raman University, Kota, Bilaspur (C.G.), India*

[2]*Asst. Professor, Department of Electronics and Communication Engineering, Dr. C. V. Raman University, Kota, Bilaspur (C.G.), India*

Abstract:** This paper presents a novel design of low-power high-speed double-tail dynamic latch comparator with SAPON tail latch. Comparators are among the key components in such systems which include zero crossing detectors, data acquisition circuits, and data converters like Analog-to-Digital Convertors (ADCs). All modern devices employing Latch Comparator (LC) should be efficient in terms of speed and power. Dynamic Latch Comparator (DLC) is one of the solutions for such efficient applications. Therefore, in this paper, a novel design of low-power high-speed double-tail dynamic latch comparator (DTDLC) is proposed with SAPON tail latch. Simulation is done with Mentor Graphics' Tanner EDA tools v2019.2 using 45nm CMOS technology. The proposed DTDLC design when operated with 1.0V supply and 100MHz clock frequency, shows a power consumption of 3.005 µWatt (which illustrates a 90.21% reduction) with time delay (clock-to-output) of 20.69 n-sec (which is 0.86% less) & PDP of 62.07 f-joule (which is 90.3% less) compared to that of a conventional DTDLC design. To verify the superiority of our proposed design in DTDLCs, existing DTDLCs are also simulated with same technology and a table is drawn for performance analysis based on parameters of power consumption, time delay, power-delay-product (PDP), and area (in terms of number of transistors used).

***Keywords:** Comparator, Static Latch Comparator, Dynamic Latch Comparator, DTDLC.*

I. INTRODUCTION

In this modern world, with the advancement of technology, the demand for power & speed efficient devices has been increased. Today, most devices in the field of communication, medical, and technology which require the applications of zero crossing detectors, data acquisition circuits, and data converters like the analog-to-digital converter (ADC), employs comparators (COMPs) as their primary structural component. In ADCs, the COMP plays a crucial role on the overall performance. [1]-[9].

A COMP compares the input signal with the reference voltage signal and generates a digital output. The COMP must be capable of finding even a small difference between the input signal and reference signal. [1]-[4], [10].

There are two types of comparators namely, Open-loop comparators and Regenerative or Latch comparators; [3]. Open loop comparators are basically Operational Amplifiers (OP-AMPs) without a feed-back; whereas, regenerative or latch comparators (LCs) use positive feed-back mechanism to compare two signals.

Earlier, COMP models were designed using OP-AMPs [10]; as shown in Fig.1. Today also, many applications use OP-AMP as an open-loop voltage comparator, but this method is generally not accurate and leads to slower performance [10]. Hence, now-a-days, the latch comparators (LCs) designed using metal-oxide semiconductor field effect transistors (MOSFETs) or Complementary MOSFETs (CMOS) are preferred. [3].

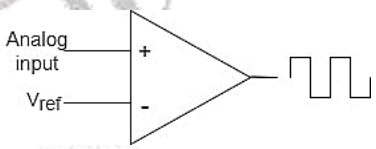

Fig.1. Block Diagram of an OP-AMP Comparator

LC uses a positive feedback mechanism (regenerative latch) which helps to increase the speed-of-operation by instantly increasing a small-scale voltage difference at the input terminals to a full-scale digital level. Thus, this mechanism regenerates the analog input signal into a full-scale digital output, enabling faster output transition with less power consumption compared to linear amplifiers; [2].

An LC is designed with following functional pins [10], as shown in Fig.2:

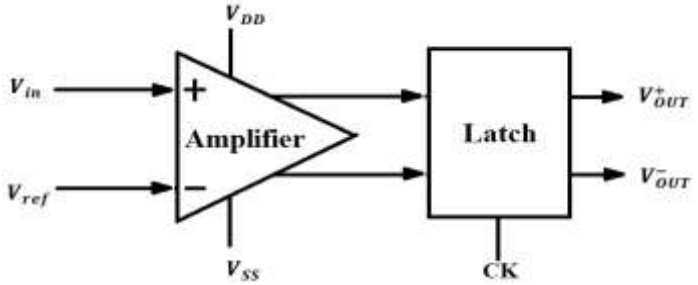

Fig.2. Functional pins of a Latched Comparator

Input Pins: the clock input (*CK*), the data signal (V_{in}) as non-inverting signal, the reference signal (V_{ref}) as inverting signal, the supply voltage (V_{DD}) as positive supply, and the supply voltage (V_{SS}) as negative supply.

Output Pins: the non-inverted output (V_{OUT}^{+}) and the inverted output (V_{OUT}^{-}).

Functionally, an LC can be defined with the following cases:

Case 1: When $CK > 0$ *and* $V_{in} < V_{ref}$;

When clock (CK) is high and input signal (V_{in}) is lower than the reference signal (V_{ref}); then non-inverted output (V_{OUT}^{+}) will be lower, equal to the negative supply (V_{SS}); while inverted output (V_{OUT}^{-}) will be higher, equal to positive supply (V_{DD}). Therefore, $V_{OUT}^{+} = V_{SS}$ & $V_{OUT}^{-} = V_{DD}$.

Case 2: When $V_{in} > V_{ref}$ *and* $CK > 0$;

When clock (CK) is high and input signal (V_{in}) is higher than the reference signal (V_{ref}); then non-inverted output (V_{OUT}^{+}) will be higher, equal to the positive supply (V_{DD}); while inverted output (V_{OUT}^{-}) will be lower, equal to the negative supply (V_{SS}). Therefore, $V_{OUT}^{+} = V_{DD}$ & $V_{OUT}^{-} = V_{SS}$.

Case 3: When $CK = 0$;

When clock (CK) is low i.e., 0; then no outputs are obtained. Therefore, V_{OUT}^{+} & $V_{OUT}^{-} = 0$.

LC Circuit models can broadly be classified in two: Static and Dynamic. [3].

Static Latch Comparator (SLC) is one which includes threshold detection based on input reference signal without any clocking mechanism. SLC models are found to be simple and quite easy to design but found no application in modern world's high-speed ADCs. Earlier designs employing static comparators suffer from high power dissipation problems because they are static, always in ON state; also, they are sluggish and less stable due to the absence of a feedback path. [3].

When compared with SLCs, positive feedback and dynamic bias are used by dynamic latched comparators (DLCs), which leads to their increased speed and reduced static power usage; [5].

1.1 DYNAMIC LATCH COMPARATOR (DLC)

Dynamic or clocked comparators obtain a very low power dissipation and at an inactive state they are turned off. DLCs are electronic blocks that only perform the comparison and provide an output after the transition of the clock. [4].

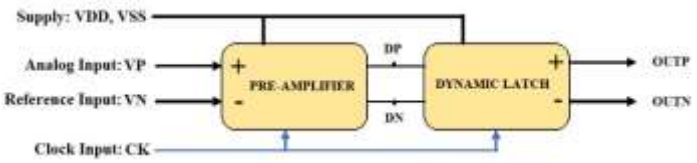

Fig.3. Block diagram of the CONV-DLC

Fig.3 gives the block diagram of a conventional dynamic latch comparator (CONV-DLC) [17]. The DLC consists of a preamplifier stage and a dynamic latch stage; [2]-[17]. A preamplifier is used to increase the resolution of the DLC but at the cost of increase in power. These clocked comparators primarily employ dynamic latches to minimize the static power consumption. When designed properly, the latches also boost the gain of the comparator and reduce the delay at low supply voltages [15].

1.2 WORKING OF CONV-DLC

A CONV-DLC has two phases of operation [1]-[17]:

(1) Reset Phase, and (2) Evaluation Phase.

During reset phase (i.e., when clock *CK* is '0' low), the output nodes of the preamplifier stage will be charged to VDD i.e., pre-charge phase, and discharge the output nodes of latch to low i.e., VSS or ground (GND).

When a *CK* signal goes from low to high (evaluation phase), the preamplifier will amplify the input difference. As soon as input reached to a distinguishable value, the positive feedback in the dynamic latch will enhance the speed and provide the differential output V_{OUTP} and V_{OUTN}. Thus, at the reset phase (*CK*=0) the output is pre-charged to logic "1". The output is evaluated at the regeneration phase (*CK*=1).

1.3 TYPES OF DLC

Architecturally, DLCs are categorized into single tail (STDLC) and double tail dynamic latch comparators (DTDLC).

STDLC consist of a differential pair with a tail current source which is connected to a regenerative latch at the output. While simple and compact, they suffer from large offset voltage and high kickback noise. They also require a large settling time, particularly at low supply voltages [8].

On the other hand, DTDLCs exhibit better performance at low supply voltages. DTDLC has two discrete stages for the input and for the regenerative latch; allowing the designer to reduce the supply voltage and optimize each stage independently for critical performance metrics such as the speed, delay, and input offset voltage; [3]. The first stage has a small tail current source to achieve low offset. The second stage (i.e. latch) has a large tail current source to provide a short delay. The presence of the second tail current source allows for faster charging and discharging of the current, further reducing the delay of the comparator. The bottom tail is used as the input stage and the upper stage is used for the latching purpose. The additional devices from the input and the regenerative stage, create a barrier between the output and input of the comparator and reduce the kickback noise. [3]. The schematic of a conventional DTDLC (CONV-DTDLC) is shown in Fig.4 of section-II.

Kick-back noise is a drawback in low-power fast-decision latched comparators. This is because a large voltage variation on the regeneration nodes of the latched comparator is coupled to the input nodes of the comparator, through the parasitic capacitances of MOSFETs; [10]. One of main methods to decrease the kick-back noise is isolating the input nodes. This idea is used in DTDLCs to increase speed in the latch stages; [10].

The input offset voltage of a comparator is the input voltage at which output changes from one logic level to the other. Or the voltage that must be applied between the two input terminals of the comparator to obtain zero volts at the output. It may be low or high, caused by device mismatch or may be inherent to the design of a comparator. [10].

In this article, a novel design of low-power high-speed DTDLC is proposed. To avoid any mismatch; and thus kick-back noise & input offset voltage problems; we have simulated all

designs with similar sizes transistors. This also helps in achieving our goal; and makes, comparison of our proposed design model with others, easier. The proposed design of DTDLC is carried out by modifying the dynamic latch stage of Chengze et. al [16] with SAPON transistors MTP & MTN of [18] while retaining the pre-amplifier stage as of CONV-SAFF [1]. Simulation is done in *45nm CMOS* technology with the help of Mentor Graphics' Tanner EDA tools *v2019.2*.

To verify the superiority of our proposed design in DTDLCs, existing DTDLCs are also simulated with same technology and a comparison table is drawn, for performance analysis, based on parameters of power consumption, time delay, power-delay-product (PDP), and area (in terms of number of transistors used).

The rest of the paper is organized as follows: in Section (II) Literature Survey; in Section (III) Proposed Design; in Section (IV) Performance Analysis; and finally, Section (V) draws Conclusion and Future Scope.

II. LITERATURE SURVEY

First, we have discussed the working of the circuit of conventional DTDLC (CONV-DTDLC) and then discussed the various improvements carried out in this design in recent years.

2.1 CONVENTIONAL DTDLC

Fig.4 represents the schematic diagram of a conventional double-tail dynamic latch comparator (CONV-DTDLC) [1].

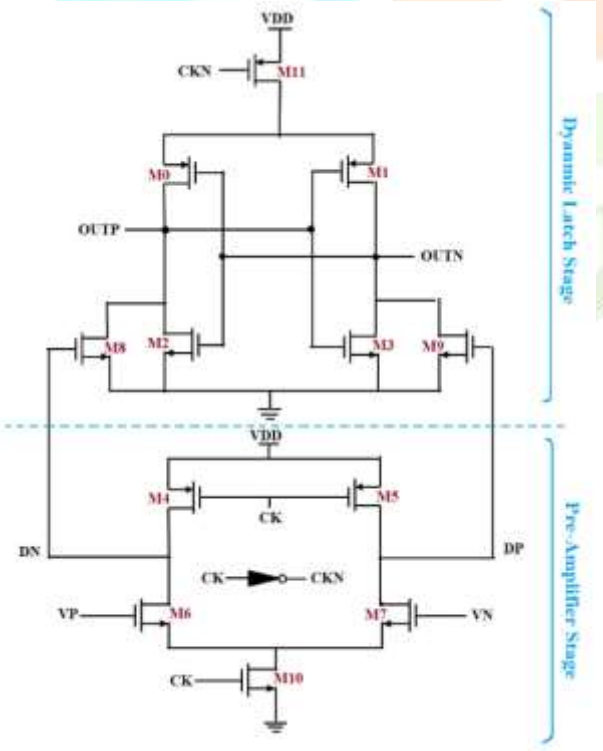

Fig.4. Schematic of CONV-DTDLC

CONV-DTDLC circuitry is a combination of two stages: Pre-amplifier stage i.e., the input stage and Dynamic latch stage i.e., output stage [1]-[17]. This two-stage structure has several advantages, including lower kickback noise, better suitability for low-voltage operation and more flexible trade-off between speed and offset [10].

As DTDLC is a CMOS based design [1]-[17], a combined circuitry of NMOS and PMOS types; hence, NMOS is ON for gate input '1' while PMOS is ON for gate input '0' [18]. Considering Fig.4, the operation of the CONV-DTDLC circuit is discussed with similar functional cases of LCs of Section-I:

Case 1: When $CK = 0$;

During reset phase when *CK=0*, M4 and M5 are ON, and M10 and M11 are OFF. Therefore, nodes *DN* and *DP* are charged to *VDD*, which causes nodes *OUTP* and *OUTN* to discharge to the ground (GND) via M8 and M9, respectively [17]. Thus, for *CK=0*, $OUTP$ & $OUTN = 0$.

In the comparison phase, when *CK=VDD*, M10 and M11 are ON, and M4 and M5 are OFF. Nodes *DN* and *DP* starts to discharge with two different discharging currents, depending on the corresponding input voltage (*VP* and *VN*). The voltage difference between *DN* and *DP* builds up the initial differential voltage at the output nodes (*OUTP* and *OUTN*), which is further amplified by the strong positive feedback of the cross-coupled latching structure. [17]

Case 2: When $CK > 0$ and $VP < VN$;

In this case, DP is pulled-down faster to GND (compared to DN) via M7 & M10, turns M9 OFF; whereas DN will be HIGH than DP, thus making M8 ON which pulls-down OUTP to GND (i.e., OUTP=0 or VSS) and the inversion circuit of M1 & M3 provides OUTN as invert of OUTP (i.e., OUTN=VDD) [17]. Therefore, $OUTP = 0$ & $OUTN = V_{DD}$.

Case 3: When $CK > 0$ and $VP > VN$;

In this case, DN will be pulled-down faster to GND (compared to DP) via M6 & M10, thus making M8 OFF; whereas DP will be HIGH than DN, thus making M9 ON which pulls-down OUTN to GND (i.e., OUTN=0) and the inversion circuit of M0 & M2 provides OUTP as invert of OUTN (i.e., OUTP=VDD) [17]. Therefore, $OUTP = V_{DD}$ & $OUTN = 0$.

This is the working of CONV-DTDLC.

2.2 IMPROVISED DTDLC

As DTDLC circuitry is a combination of Pre-amplifier stage and Dynamic latch stage. Variations are done in these to improve the performance of the design. Here, we have discussed some of the important improvements carried out in recent years for designing low power models of DTDLC.

Khorami A. et al. [6] proposed a low power technique for Dynamic Comparators in which, the pre-amplification phase is stopped when there is enough differential voltage at the output of the latch stage to avoid excess operation of the pre-amplifier, hence, reduces the power consumption. Therefore, an XOR gate is used to check whether the output differential voltage of the latch is large enough and controls the power supply for pre-amplifier. The schematic of the proposed design is shown in Fig.5.

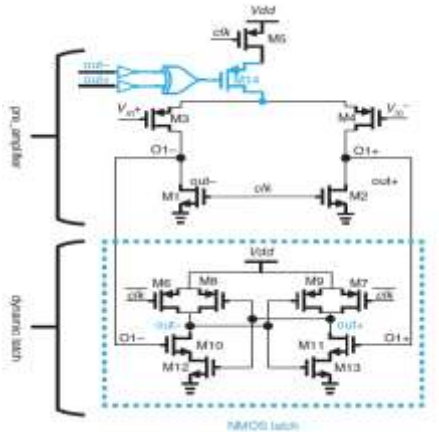

Fig.5. Khorami's XOR gate Dynamic Latch Comparator

Although, the proposed modification helped in controlled power supply to the circuit but it increased the area and the delay due to the increased number of transistors.

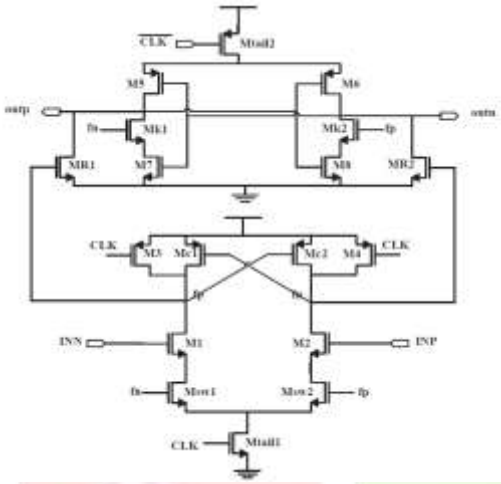

Fig.6. Jain's DTDLC

Jain R. et. al [7] observed that the total delay time of DTDLC is dependent on the latch effective trans-conductance and the output difference voltage. Thus, the proposed DTDLC exploits this dependence of latch regeneration time on the output difference voltage. By adding two key transistors *MK1-MK2* to the latch circuit the effective trans-conductance of intermediate stage transistors is enhanced. This in turn enhances output difference voltage which leads to increased latch regeneration speed or reduced delay time. The proposed DTDLC is shown in Fig.6.

Although the proposed design reduced the total delay but the power reduction is not achieved satisfactorily and is also not clearly mentioned in their paper work.

Varshney V. et al. [8] proposed a power-efficient low-offset dynamic latch comparator, which is basically a modified version of double tail dynamic latch comparator (DTDLC). The schematic of the proposed design is shown in Fig.7.

In this proposed design, the difference outputs of pre-amplifier (here, Fp & Fn) are directly fed to the source nodes of latch stage transistors, which makes the design more robust against mismatch and process variations, and results lesser input offset voltage without penalty on power and speed. Also, the outputs of latch are controlled by clock driven transistors (M9 & M10) to further save power.

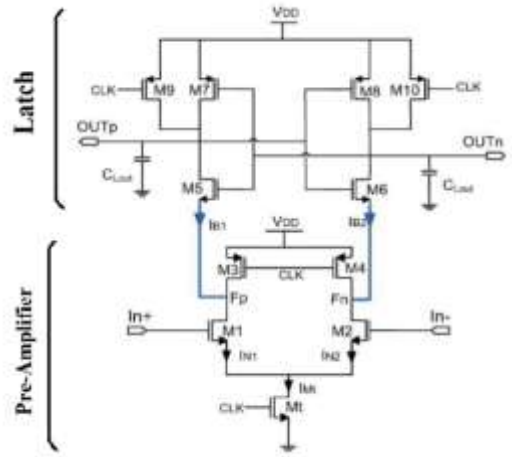

Fig.7. Varshney's DTDLC

Although, this design effectively reduced the power consumption but the delay is enhanced.

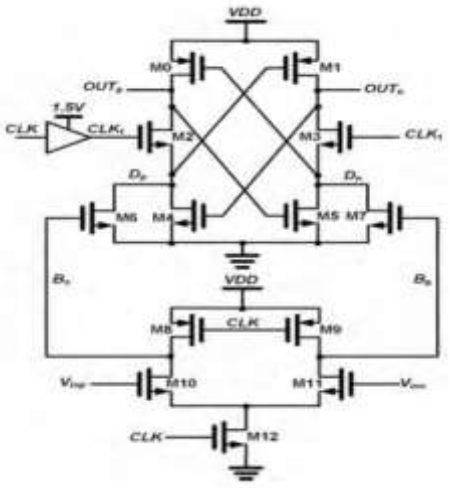

Fig.8. Wang's DTDLC

Wang Y. et al. [9] observed that, mostly dynamic comparators use a pair of cross-coupled inverters as the latching stage, which provides strong positive feedback, to accelerate the comparison and reduce the static power consumption. However, at the beginning of the comparison phase, the conventional latching stage has two transistors with zero gate-to-source voltage, which degrade the total effective transconductance of the latching stage. And the delay of the comparator is mainly determined by the total effective transconductance of the latching stage.

Therefore, authors proposed a low-power high-speed DTDLC with a transconductance-enhanced latching stage, as shown in Fig.8. The proposed latching stage uses separated gate-biasing cross-coupled transistors instead of the conventional cross-coupled inverter structure. This simple proposed latching stage improves its effective total transconductance at the beginning of the comparison phase, which leads to a much faster comparison.

Although, this proposed design reduced the delay but the power consumption is increased.

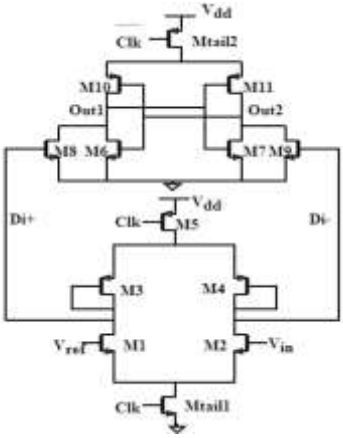

Fig.9. Fernandes' DTDLC

Fernandes J. M. et al. [10] proposed a modified DTDLC with reduced glitches for low frequency applications. The power is dissipated only in regeneration phase (CLK=1) of the comparator which reduces the total power consumption. Therefore, in the proposed design, instead of clock driven input transistors of the pre-amplifier stage, the diode connected transistors (M3 and M4) are inserted between the input transistors. This reduces the output swing from (VDD to 0) to [(VDD-VDS) to 0]. Hence, reduces the dynamic power dissipation. This also reduces the delay of the circuit. The proposed design is shown in Fig.9.

Although, this proposed design is fast because of effective reduction in delay but reduction in power consumption achieved is not pleasing and is near to that of CONV-DTDLC.

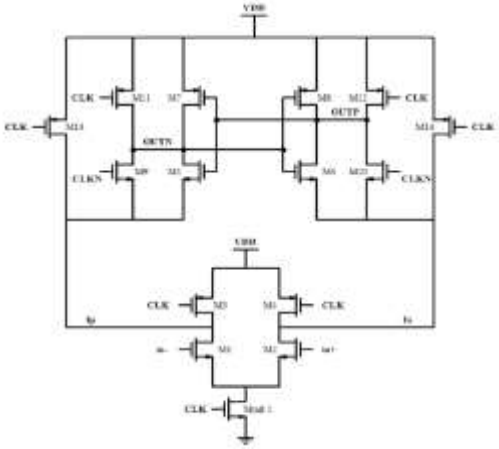

Fig.10. Yousefi's DTDLC

Yousefi et al. [11] proposed a low-power DTDLC in which pre-amplifier stage difference outputs (here, fp & fn) are directly latched to outputs (OUTN & OUTP, respectively) through clock-inversion driven transistors. Because of this direct coupling to latch, effective reduction in power consumption is achieved. This proposed design is shown in Fig.10.

Although, this proposed design is power efficient but delay is increased due to additional clock driven transistors.

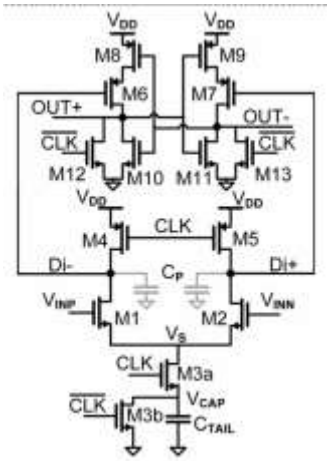

Fig.11. Chengze's DTDLC

Chengze et al. [16] proposed a novel DTDLC design, as shown in the Fig.11, in which two transistors are used at the tail of pre-amplifier, first is driven with clock and second with clock-inversion signal in-parallel with a capacitor to make the difference voltage (±Di, here) discharging slower and with clock-controlled. And in the dynamic latch stage, these difference voltage signals are fed to the gate of transistor (M6,7) between the inverter circuit of output signals (OUT±) of dynamic latch. These transistors effectively control the output signals and makes the design power efficient and fast.

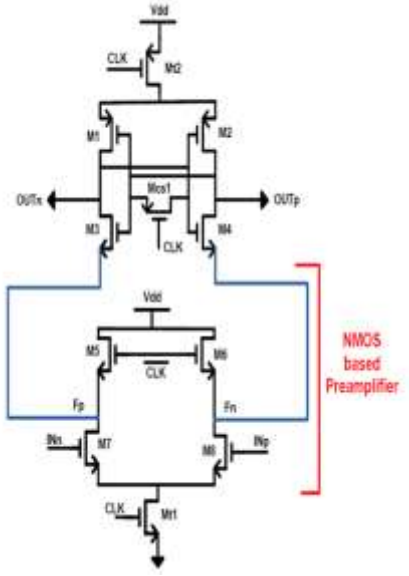

Fig.12. Saxena's DTDLC

Abhinav Saxena et al. [17] proposed an energy-efficient low-power dynamic comparator which is a modified version of double tail dynamic latch comparator (DTDLC). To improvise dynamic comparator, modification is carried out in the pre-charge step (for CK = 0) and the regeneration step (for CK > 0), the two primary steps in the operation of the dynamic comparator. The preamplifier stage is designed using NMOS transistors only which enables the circuit to have faster comparison speed and lesser power consumption. And in the latch stage, a PMOS pass transistor (Mcs1) is utilized which incorporates the charge sharing concept in the regeneration step, which reduces power consumption. The schematic of their proposed DTDLC is shown in Fig.12.

Although, this proposed design is power-efficient but the increased delay is its drawback.

So, these are the important improvements carried out in the

recent years in the field of low-power high-speed DTDLC design.

III. PROPOSED DTDLC

We propose a novel design of low-power high-speed DTDLC with SAPON tail latch. The proposed DTDLC design model is composed by modifying conventional DTDLC [1], in which the dynamic latch stage is replaced with that of Chengze's DTDLC [16] employed with SAPON transistors MTP & MTN of [18] while retaining the pre-amplifier stage.

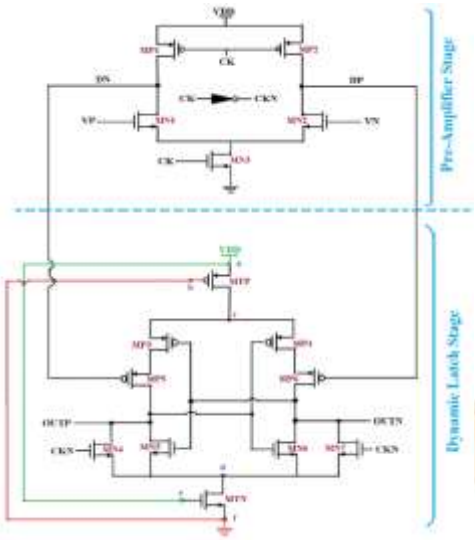

Fig.13. Schematic of Proposed DTDLC

3.1 SAPON TECHNIQUE IN DTDLC:

Switching and short-circuit leakage power plays a significant role in the high-frequency dynamic transition of inputs. To lessen power consumption of the CMOS based logic circuit, [18] proposed a new power reduction technique calling it the SAPON i.e., Stackly Arranged low Power ON transistor technique. As per authors, SAPON provides better power reduction than existing standard reduction techniques.

In this technique, the SAPON transistors MTP (PMOS-type) & MTN (NMOS-type) are connected in series between the supply (V_{DD}) and the ground (GND) which is V_{SS}, while their gates are wired with GND and V_{DD}, respectively. These SAPON transistors MTP & MTN functions in a fashion that they remain active during working phase but cuts-off the supply of the circuit during the leveling i.e., the transition phase. This helps to reduce the power consumption, because during the leveling i.e., transition phase, when all PMOS switching from HIGH to LOW and all NMOS switching from LOW to HIGH; for a short period all PMOS & NMOS of the circuit conducts, creating a short-circuit path for current flow which is an undesirable leakage of current. So, to prevent this leakage of current in the circuit, SAPON transistors play a vital role and cut-off the supply from the circuit under such situation. In this way by reducing the leakage current this technique also reduce the power consumption of the circuit. Consequently, it produces desired results while yet using little power.

The purpose of SAPON technique in DTDLC is to minimize the power consumption of the circuit in the similar fashion. For the working of SAPON in DTDLC, consider the dynamic latch stage of Fig.13. When logic '1' is given as input to the gate terminal of NMOS (MTN), it will turn ON and when logic '0' is given as input to the gate terminal of PMOS (MTP), it will turn ON; hence to make these transistors active during working phase, wired path ae=1 is supplied to MTN with V_{DD} connection and wired path fb =0 is supplied to MTP with GND connection. In this way, initially, both MTP AND MTN are in ON state.

During transition period when all NMOS & PMOS conducts creating a short circuit path from V_{DD} to GND, therefore logic '1' reaches at node 'd' of MTN. As MTN is in ON state because node 'e' at its gate, is wired to VDD; the logic '1' reaches to node 'f' and thus, through path 'fb', logic '1' is applied on MTP which turns PMOS (MTP) to OFF which cut-off the supply V_{DD} from the circuit. In this way, SAPON arrangement cut-off the short-circuit leakage current in the DTDLC circuit and prevents the power consumption during the leveling i.e., transition phase.

In this way, SAPON technique helps to reduce power consumption in proposed DTDLC, making it a low-power design.

3.2 PROPOSED DTDLC WORKING

Consider Fig.13 of the proposed DTDLC design. The operation of the proposed DTDLC circuit is discussed with following similar cases as of CONV-DTDLC:

Case 1: When $CK = 0$;

During the reset phase when *CK=0*; MP1 and MP2 are ON making nodes DN & DP charged to V_{DD} which turns OFF MP5 & MP6 and cuts off the cross-coupled inversion circuits (MP3-MN5 & MP4-MN6). Meanwhile *CKN=1* which causes output nodes *OUTP* and *OUTN* to discharge to the V_{SS} i.e., ground (GND) via MN4-MTN and MN7-MTN, respectively. Thus, making $OUTP$ & $OUTN = 0$ i.e., V_{SS}. Therefore, $OUTP$ & $OUTN = 0$ i.e., V_{SS}.

In the comparison phase, when *CK=1*; MN3 is ON, and MP1 and MP2 are OFF. Nodes *DN & DP* starts to discharge with two different discharging currents, depending on the corresponding input voltages (*VP and VN*) and turns ON the corresponding transistors MP5 & MP6 of the dynamic latch stage; which will complete i.e., turns ON the cross-coupled inversion circuits (MP3-MN5 & MP4-MN6). Meanwhile *CKN=0*, MN4 & MN7 are OFF. The difference in voltage between *DN* and *DP* builds up the differential voltage at the output nodes (*OUTP* and *OUTN*) via the cross-coupled inversion circuits.

Case2: When $CK > 0$ and $VP < VN$;

In this case, DP will be pulled-down faster to GND (compared to DN) via MN2 & MN3, thus making MP6 ON "faster" compared to MP5. Due to this, the inversion circuit (MP4-MN6) firstly inverts the present input signal (i.e., the previous value) of *OUTP*; which is generally '0' due to CK=0 in previous pulse; to give the output *OUTN* as '1' i.e., V_{DD} and then the other inversion circuit (MP3-MN5) will invert this current value of *OUTN* to give the output *OUTP* as '0' i.e., V_{SS}. So, if $CK > 0$ and $VP < VN$; then firstly $OUTN$ and then $OUTP$ gives the inversion outputs. Therefore, $OUTP = 0$ $i.e.,V_{SS}$ & $OUTN = V_{DD}$.

Case 3: When $CK > 0$ and $VP > VN$;

In this case, DN will be pulled-down faster to GND (compared to DN) via MN1 & MN3, thus making MP5 ON "faster" compared to MP6. Due to this, the inversion circuit (MP3-MN5) firstly inverts the present input signal (i.e., the

previous value) of *OUTN*; which is generally '0' due to CK=0 in previous pulse; to give the output *OUTP* as '1' i.e., V_{DD} and then the other inversion circuit (MP4-MN6) will invert this current value of *OUTP* to give the output *OUTN* as '0' i.e., V_{SS}. So, if $CK > 0$ *and* $VP > VN$; then firstly $OUTP$ and then $OUTN$ gives the inversion outputs. Therefore, $OUTP = V_{DD}$ & $OUTN = 0$ i.e., V_{SS}.

This is how our proposed DTDLC works.

IV. SIMULATION & RESULT COMPARISON

The proposed DTDLC has been designed based on *45 nm CMOS* technology. In order to verify the validity of the proposed DTDLC and comparison of result, CONV-DTDLC and other DTDLCs have also been designed in same technology. To avoid any mismatch; and thus kick-back noise & input offset voltage problems; we have simulated all designs with similar sizes transistors. This also helps in achieving our goal; and makes comparison between designs easier. Simulation is carried out in Mentor Graphics' Tanner EDA tools *v2019.2*. Using W/L of all NMOS= *230/50nm* and of all PMOS= *530/50nm* in each design for simulation and the output results.

T-SPICE with the same settings is adopted to perform all post-layout simulations for comparison. The performance comparisons such as of the average power consumption, CK-to-Q delay, power-delay product (PDP), and area (in terms of number of transistors used) are described in Table. I.

Settings used are:

Clock: CK=Pulse Signal of ON=1.2V & OFF=0V, 100MHz;

Power Supply: V_{DD} = 1.0V, V_{SS} = 0V i.e., ground GND;

Input Signal at Non-inverting Node: VP= SINE (250mV, 5MHz);

Input Signal at Inverting Node: VN= DC (150mV);

Scaling Used: NMOS: W=230n L=50n; PMOS: W=530n L=50n;

Measuring Clock-Output Delay: trigger V(CK) for value=0.5 on rise=1st and target V(OUTP) for value=0.5 on rise=1st.

4.1 SIMULATED DESIGNS AND THEIR WAVEFORMS

Here, we have shown the simulated designs of only the CONV-DTDLC [1], Chengze's DTDLC [16] (whose latch is employed in the Proposed design), and the Proposed DTDLC to compare their properties via transients' waveform and output waveforms. While other DTDLCs are compared with the Proposed DTDLC based on the performance metrics shown in Table. I of Section 4.2: Performance Analysis.

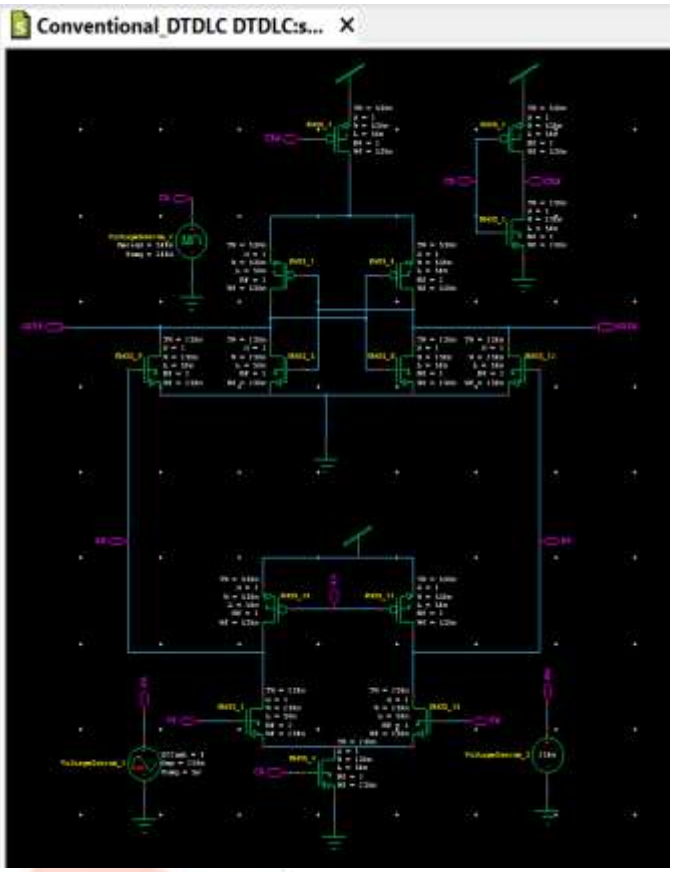

Fig.14.1 Simulated Schematic of CONV-DTDLC

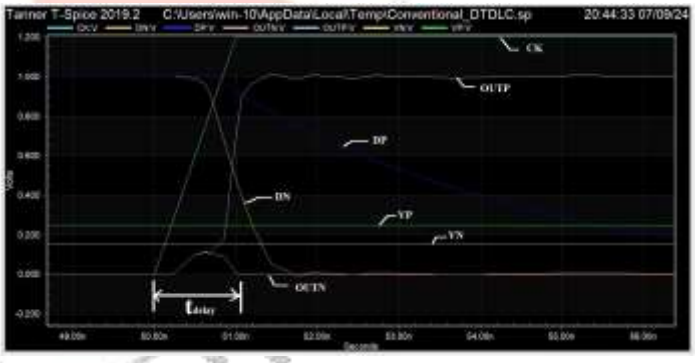

Fig.14.2 Transient Simulation of CONV-DTDLC

It is clear from transient simulation of CONV-DTDLC, as shown in Fig.14.2, during evaluation phase when clock CK turns from LOW-to-HIGH and $VP > VN$, leading to discharge of DN 'faster' than DP; and hence, OUTN initially rises with OUTP and after output process delay (t_{delay}), OUTN falls to zero '0' i.e. V_{SS} while OUTP rises to V_{DD} , performing its operation as a latch comparator. The output delay time (t_{delay}) observed with CONV-DTDLC is large.

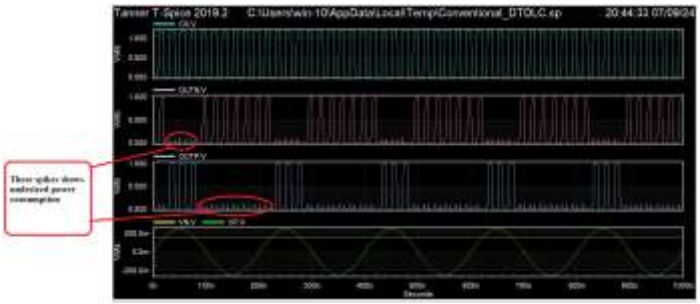

Fig.14.3 Output Waveform of CONV-DTDLC

In the output waveform of CONV-DTDLC, as shown in Fig.14.3, high spikes are observed which symbolizes undesired output power consumption.

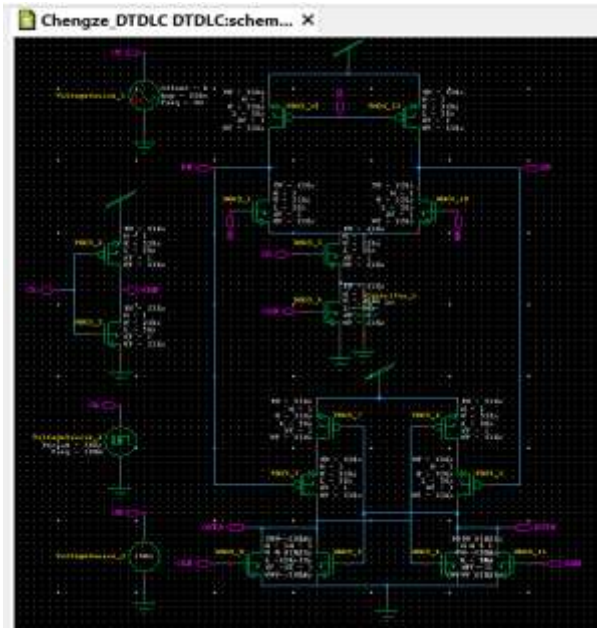

Fig.15.1 Simulated Schematic of Chengze's DTDLC

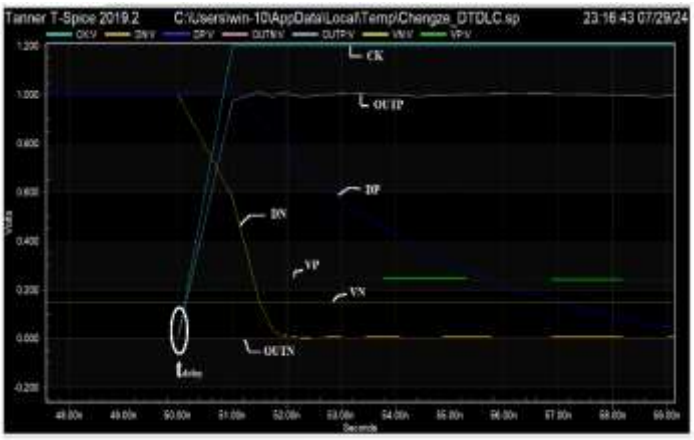

Fig.15.2 Transient Simulation of Chengze's DTDLC

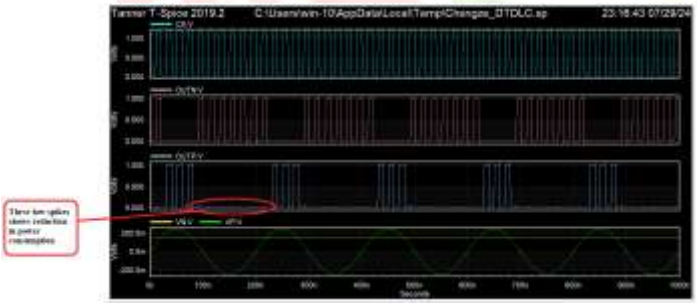

Fig.15.3 Output Waveform of Chengze's DTDLC

From Fig.15.2 & Fig.15.3, it is clear that, Chengze's DTDLC design has low output delay and low power consumption. Hence, its latch is employed in our proposed design.

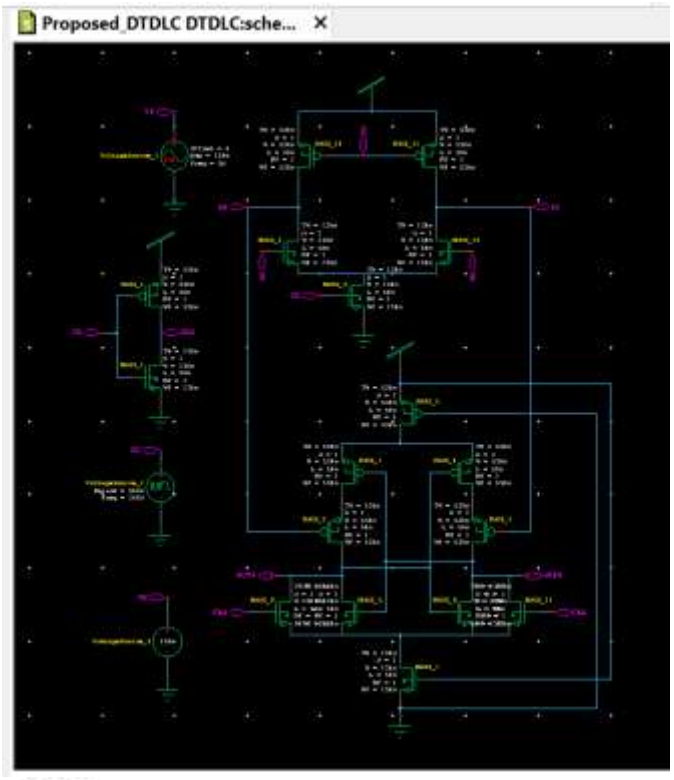

Fig.16.1 Simulated Schematic of Proposed DTDLC

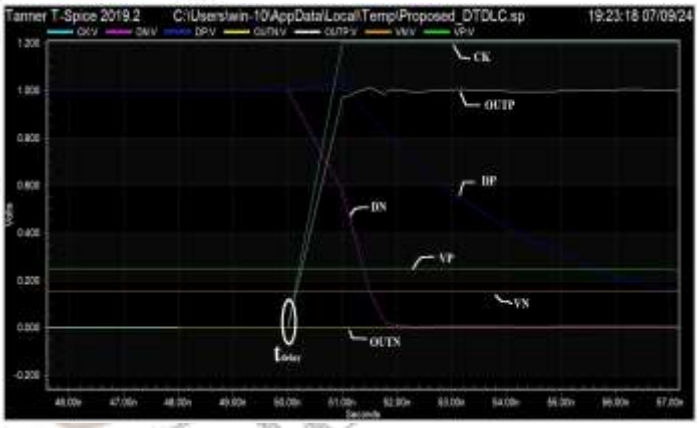

Fig.16.2 Transient Simulation of Proposed DTDLC

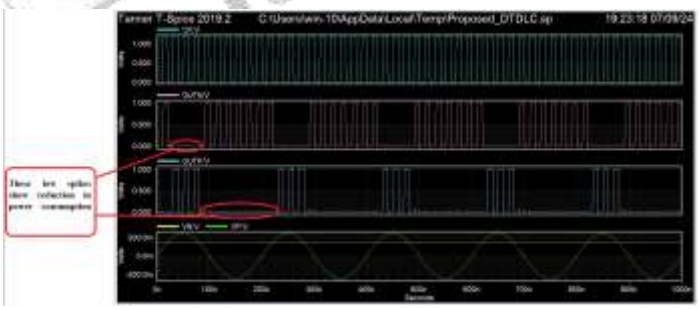

Fig.16.3 Output Waveform of Proposed DTDLC

It is clear from transient simulation of Proposed DTDLC, as shown in Fig.16.2, for the same evaluation phase its output delay time (t_{delay}) is very less compared to CONV-DTDLC.

In the output waveform of Proposed DTDLC, as shown in Fig.16.3, low spikes are observed which symbolizes reduced undesired output power consumption.

4.2 PERFORMANCE ANALYSIS

In this section, performance of the various discussed designs is evaluated by drawing a table based on average power consumption, clock-to-output delay time, power-delay-product (PDP), and area (in terms of no. of transistors used); when all others are designed with same technology and settings used as of the proposed design. Table. I show the Performance Analysis of DTDLCs.

Table. I. Performance Analysis of discussed DTDLC models and the Proposed DTDLC

DTDLC with schematic	AVERAGE POWER CONSUMED	DELAY (CK-OUTP)	POWER-DELAY PRODUCT (PDP)	AREA (No. of Transistors)
CONV_DTDLC [1] Fig. 12(a)	P = 3.071626e-05 watt = 30.72 µ-watt (× 1) Max power = 2.763268e-04 at time = 4.05e-08 Min power = 9.258384e-08 at time = 1.79199e-08	D = 20.8761n-sec = 20.87 n-sec (× 1)	|PDP| = 641.13 f-J (× 1)	14
JAIN DTDLC (2017) Fig. 12(f)	P = 3.434260e-05 watts = 34.34 µ-watt (× 1.12) Max power = 1.988089e-04 at time = 9.20513e-07 Min power = 3.753496e-08 at time = 2.80875e-07	D = 21.3854 n-sec = 21.38 n-sec (×1.02)	|PDP| = 734.2 f-J (×1.14)	15
VARSHNEY DTDLC (2018) Fig. 12(g)	P = 5.225048e-06 watt = 5.23 µ-watt (×0.17) Max power = 2.785287e-04 at time = 4.06596e-08 Min power = 9.296457e-07 at time = 2.66e-07	D = 30.0564 n-sec = 30.06 n-sec (× 1.44)	|PDP| = 157.21 f-J (×0.24)	13
WANG DTDLC (2019) Fig. 12(b)	P = 6.732065e-05 watt = 67.32 µ-watt (×2.19) Max power = 5.621305e-04 at time = 6.40584e-07 Min power = 1.506115e-07 at time = 2.07362e-08	D = 10.0861 n-sec = 10.1 n-sec (× 0.48)	|PDP| = 679.93 f-J (×1.06)	17
FERNANDES DTDLC (2019) Fig. 12(f)	P = 5.173125e-05 watt = 51.73 µ-watt (×1.68) Max power = 2.687940e-04 at time = 4.05e-08 Min power = 2.952620e-07 at time = 6.8e-07	D = 5.7090 n-sec = 5.71 n-sec (× 0.27)	|PDP| = 295.4 f-J (×0.46)	15
YOUSEFI DTDLC (2020) Fig. 12(c)	P = 5.937959e-06 watt = 5.94 µ-watt (×0.193) Max power = 2.137326e-04 at time = 6.405e-07 Min power = 8.175645e-09 at time = 5.115e-07	D = 29.8331 n-sec = 29.83 n-sec (× 1.43)	|PDP| = 177.19 f-J (×0.27)	17
CHENGZE DTDLC (2022) Fig. 12(e)	P = 6.459243e-06 watt = 6.46 µ-watt (×0.21) Max power = 3.253052e-04 at time = 3.80586e-07 Min power = 1.116300e-07 at time = 7.10298e-08	D = 20.6812 n-sec = 20.68 n-sec (× 0.99)	|PDP| = 133.59 f-J (×0.21)	16
SAXENA DTDLC	P = 6.065733e-06 watt = 6.06 µ-watt (×0.197)	D = 30.1499 n-sec = 30.15 n-sec	|PDP| = 182.71 f-J	

(2023) Fig. 12(d)	Max power = 3.310087e-04 at time = 2.0589e-08 Min power = 5.289630e-07 at time = 6.1e-08	(× 1.44)	(×0.28)	13
PROPOSED DTDLC Fig. 12(g)	P = 3.005562e-06 watt = 3.01 µ-watt (×0.098) i.e., 90.2% less than CONV_DTDLC Max power = 1.205357e-04 at time = 1.00601e-07 Min power = 8.026017e-09 at time = 7.15011e-07	D = 20.6885 n-sec = 20.69 n-sec (× 0.991) i.e., 0.86% less than CONV_DTDLC	|PDP| = 62.07 f-J (×0.09) i.e., 90.3% less than CONV_DTDLC	17

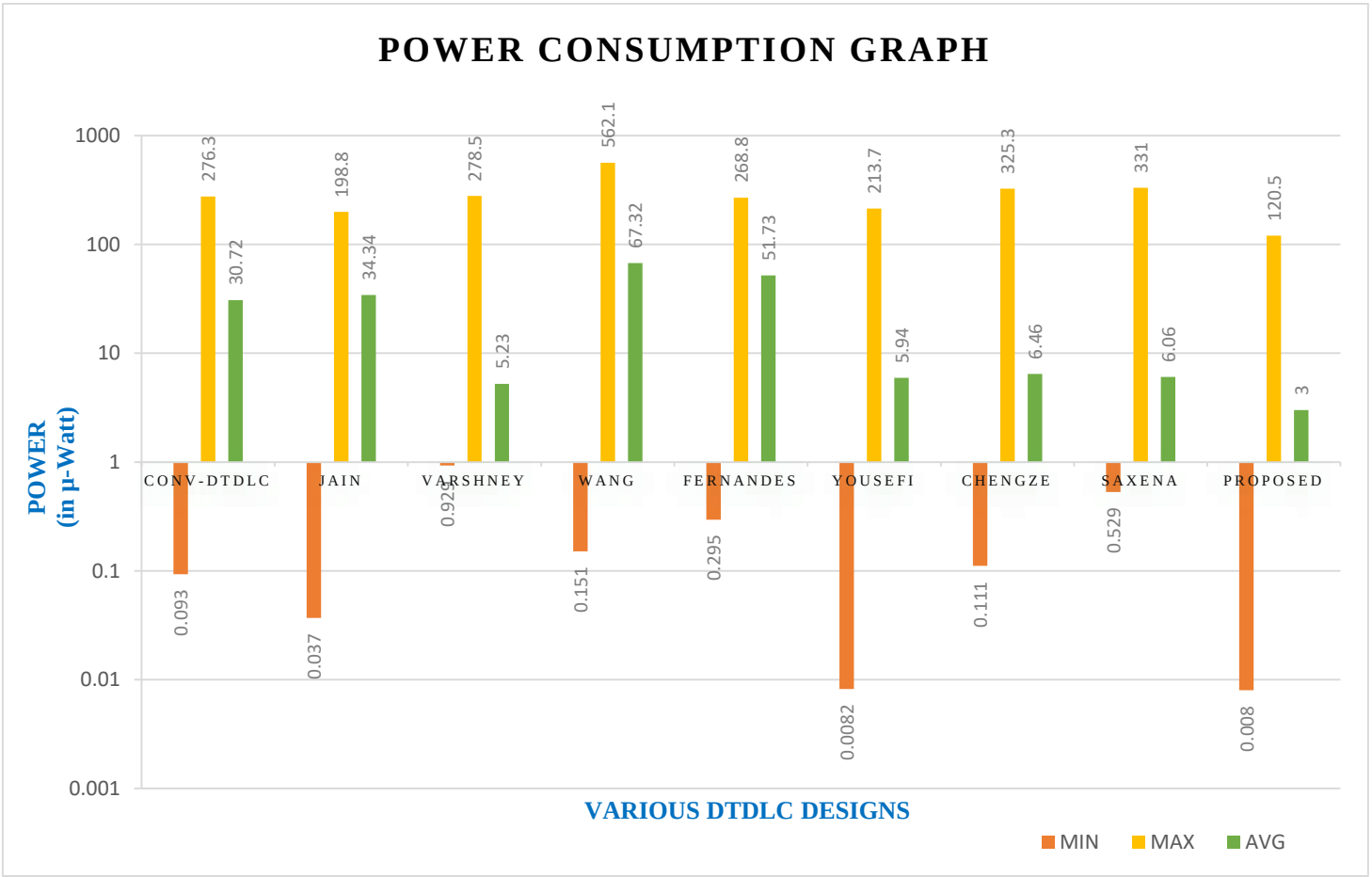

Fig.17. Power Consumption Graph of DTDLC Designs

Thus, it is clear from Table. I of Performance Analysis and Fig.17 of Power Consumption Graph of various discussed DTDLC designs that the proposed DTDLC is superior as it shows a power consumption of 3.005 µWatt (which illustrates a 90.21% reduction) with a time delay (clock-to-output) of 20.69 n-sec (which is 0.86% less) and a PDP of 62.07 f-joule (which is 90.3% less) compared to that of a conventional DTDLC design. Hence, we can say, the proposed DTDLC is a low-power high-speed design.

V. CONCLUSION & FUTURE SCOPE

This paper proposes a novel design of low-power high-speed double-tail dynamic latch comparator (DTDLC) with SAPON tail latch. The proposed DTDLC design model is composed by modifying conventional DTDLC [1], in which the dynamic latch stage is replaced with that of Chengze's DTDLC [16] employed with SAPON transistors MTP & MTN of [18] while retaining the pre-amplifier stage. The dynamic latch stage of Chengze's DTDLC when employed with SAPON transistors reduces the power consumption because SAPON arrangement cut-off the short-circuit leakage current in the DTDLC circuit and prevents the power consumption during the leveling i.e., transition phase. This makes our proposed DTDLC a low-power design. To verify

the superiority of our proposed design in DTDLCs, existing DTDLCs are also simulated with same technology and a table is drawn for performance analysis based on parameters of power consumption, time delay, power-delay-product (PDP), and area (in terms of number of transistors used). All designs are simulated in Mentor Graphics' Tanner EDA tools v2019.2 using *45nm CMOS* technology. The proposed DTDLC design when operated with 1.0V supply and 100MHz clock frequency, shows a power consumption of 3.005 µWatt (which illustrates a 90.21% reduction) with time delay (clock-to-output) of 20.69 n-sec (which is 0.86% less) & PDP of 62.07 f-joule (which is 90.3% less) compared to that of a conventional DTDLC design. All these parameters confirms that our proposed DTDLC design is a low-power high-speed model among existing designs.

In future we may carry out further reduction in its power consumption and delay by improvising the pre-amplifier stage whose tail transistor is controlled with clock (CK) only. As during the comparison phase, when the logic of CK is equal to 1 i.e., VDD, the discharge of the drain nodes DP and DN begins through this CK controlled tail transistor. This leads to complete discharge of power in DP & DN nodes. And again, charging these nodes to VDD consumes more power. So, this undesired power consumption needs to be controlled.

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AUTHORS

Satish Yadav is currently a Student of Master of Technology in VLSI Branch of Electronics and Communication Engineering Department at Dr. C. V. Raman University (CVRU), Bilaspur, Chhattisgarh State, India. Prior to this, he completed his Bachelor of Engineering in Electronics & Telecommunication Engineering from Chhattisgarh Swami Vivekananda Technical University (CSVTU), Bhilai, Durg District, Chhattisgarh State, India.

Corresponding Author.

Email ID: satish.yad100@gmail.com

Pallavee Jaiswal is Assistant Professor in the Department of Electronics and Communication Engineering, Dr. C. V. Raman University (CVRU), Bilaspur, Chhattisgarh State, India. She received her B.E. Degree in Electronics and Telecommunication Engineering From GEC, Raipur (C.G.), India & MTech Degree in Digital Communication from Dr. C. V. Raman University, Bilaspur (C.G.), India. She is pursuing her PhD in Electronics and Communication Engineering from Dr. C. V. Raman University, Bilaspur. She is UGC -NET qualified. She has more 10 Years of teaching experience. She has published more than 15 paper in the reputed journals. Her research interests cover Signal Processing, Image Processing, Speech Processing.

Email ID: pallavee10@gmail.com