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Integrating SPI And I2C Communication Protocols In A Controller Interface

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Abstract: While I2C and SPI are established communication protocols for embedded systems, their strengths cater to different applications. I2C offers a low-pin- count, multi-master design ideal for low-speed communication with numerous de- vices. SPI excels in high-speed, full-duplexdata exchange between a single master and peripherals. This paper explores integration strategies for leveraging the benefits of both protocols within an embedded system. It targets efficient implementation through synthesis using Genus and physical design using Innovus.

Index Terms **- SPI, I2C**

I. INTRODUCTION

Effective communication between micro- controllers and a wide variety of peripheral devices is essential to the eld of embedded systems. For this purpose, two popular protocols Serial Peripheral Interface (SPI)and Inter-Integrated Circuit (I2C) have become effective tools. Even though both protocols provide useful functionality, thereare many circumstances in which an embedded system can profit from both of their advantages. The integration of SPI and I2C protocols into a single system is examined. A greater range ofcommunication options can be unlocked by carefully integrating their features, creatingmore adaptable and potent embedded systems.

II. LITERATURE REVIEW

In order to improve the performance of the Serial Peripheral Interface (SPI) protocol, which is frequently used in embedded systems, this study investigates the incorporation of clock gating approaches. With this method, the clock signal is selectively disabled during the blocks' idle states, which significantly lowers power consumption while preserving dependable and fast data transfer. Our study illustrates the effectiveness of the suggested clock gating method in striking a balance between communication speed and power consumption through comprehensive calculations and experimental validations. In addition to being useful for SPI applications, this research can be used as a paradigm to optimize other communication protocols[1].

SPI was modeled in Verilog code and simulated and integrated in the early stages of design using Model-Sim and Quartus Prime Lite Edition 16.0. This article describes the design and structure of a Serial Peripheral Interface (SPI) IP core with an Enhanced Peripheral Bus (APB) interface. The SPIinterface is designed to send or receive data from a slave. SPI mode also plays a role in this eort, with the processor operating from four modes corresponding to four-time settings. The results showed that the SPI core was successfully modeled for types 0, 1, 2 and 3. The ASIC design for this project uses 27750m2 and 47.12W using the Silterra 0.18m CMOS process [2].

I2C protocol provides simple communication without data loss. It is also faster than other programs. Lightweight, economical and ubiquitous. It also increases data transfer speed. The purpose of creating this system is to provide fast communication and manage the record on the device and the information that can be stored in the record and that we can control. There are many things that do not exist. I2C is used to monitor

data to increase accuracy and efficiency. This design method is designed using VHDL simulated on MODELSIM or Xilinx and can be implemented on the FPGA board[3].

III. PROBLEM STATEMENT

Current controllers do not support SPI or I2C natively, so additional devices and software libraries must be used. This leads to an increase in board size, complexity, and development time. A single controller unit with a single software interface is what we propose doing when merging SPI and I2C modules. This improves development effectiveness, reduces costs, and streamlines design for systems that use a range of peripheral communication techniques.

IV. OBJECIVES

• Develop a controller unit with built-in SPI and I2C modules to eliminate external interface chips and unify communication protocols.

• Synthesize and implement an efficient SPI master protocol using Cadence Genus for logic synthesis and Innovus for physical design.

• Vary the floorplan ratio and power planning for better optimization

IV. METHODOLOGY

• Develop a controller unit with built-in SPI and I2C modules
• Develop comprehensive Verilog testbenches to simulate design and simulate using Xcelium simulator
• Use Genus tool to synthesize the gate level netlist and gate level circuit.
• Analyze for Area, power and timing .
• Implement the generated netlist for Physical design using Innovus tool.
• Vary the floorplan ratio and power planning for better optimization.

V. BLOCK DIAGRAM

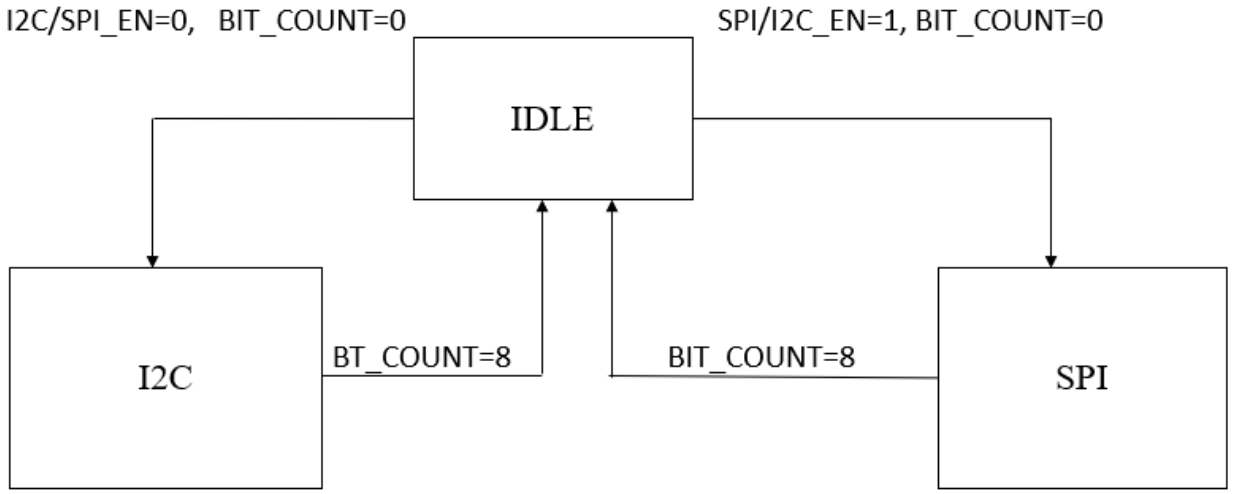

Fig 1 Controller Block Diagram

Fig 1 shows the basic block diagram of the controller block, designed for integrating SPI and I2C protocols. It consists of 3 states, namely IDLE state, SPI state and I2C state. Initially, the controller is in IDLE state. When spi/i2c-enable is active high, the control moves to SPI state and it stays in that state until all bits are transferred. Similarly, When spi/i2c-enable is active low, the controller is moved to I2C state and the data transfer begins.

VI. RESULTS AND DISCUSSION

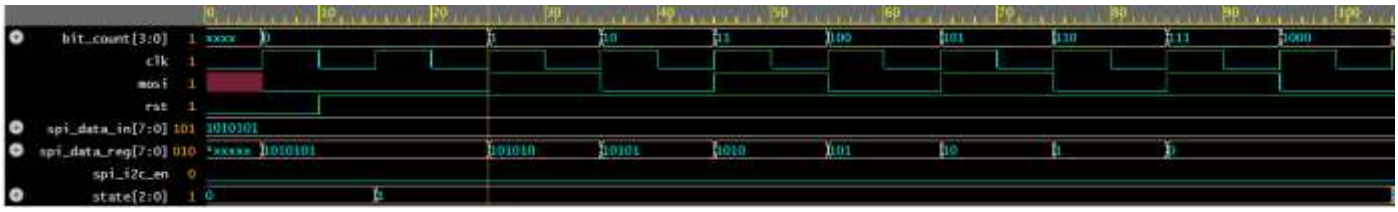

Fig 2 SPI functionality

Figure 2 shows the SPI functionality of the controller block. When SPI/I2C-enable is low, the signal bit-count starts counting the number of bits transferred.The data present in SPI-DATA-REG is tranfered one bit at a time to MISO signal which can be connected to the slave.When bit-count reaches 8, the curren state goes back to IDLE state.

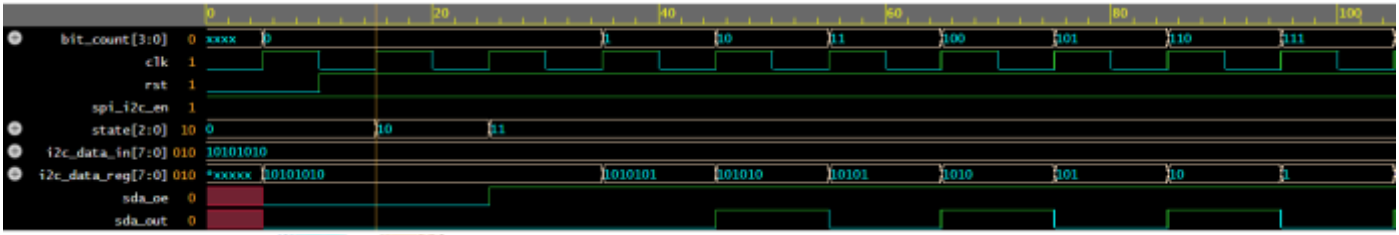

Fig 3 I2C functionality

Figure 3 shows I2C functionality of controller block. When SPI/I2C-enable is high, the data-output-enable is activated. Once it's activated, the bit-count starts counting the number of bits transferred.The data present in I2C-DATA-REG is tranfered one bit at a time to SDA signal which can be connected to the slave.

Table 1 Comparison of Reports

Parametrs	This Work	Previous work[1]
Timing	440ps	-
Power	42uW	114mW
Area	257.184um 2	-

Table 1 shows the valves of parameters Timing, Power and Area, which are obtained from Genus synthesis tool. When compared from previous papers, The power consumption has reduced significantly.

VII. CONCLUSION

VIII. The objectives outlined in this projectaim to develop a robust and efficient controller unit with built-in SPI and I2C mod- ules, unifying communication protocols andoptimizing the design for performance and power efficiency.

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