



Memristor Ratioed Logic For Low Power Encoder Design

Pramod¹, Dr. Mahesh R K²

^{1,2} Dept. of ECE, Faculty of Engineering Technology (Co-Edu.) Sharnbasva University, Kalaburagi – 585103

ABSTRACT

The emergence of memristor-based digital logic gates presents a promising alternative to conventional IC design paradigms, signaling a new era in computing architecture. Leveraging memristors for logic gate design offers simplicity in manufacturing, as memristors can be integrated atop the poly-silicon gate of NMOS transistors, facilitating increased transistor density on a chip. In this context, this work focuses on the development and analysis of a 3-bit encoder utilizing Memristor Ratioed Logic (MRL), aiming to harness its potential for low-power applications. The proposed encoder design showcases superior power efficiency compared to conventional CMOS designs, positioning it as a compelling solution for energy-conscious computing environments. By employing MRL, the encoder serves as a versatile platform for modeling various combinational logic circuits, demonstrating its efficacy in diverse computational tasks. The primary objective of this work is to design and analyze a 3-bit encoder employing various logical methodologies, utilizing LTspice for simulation and evaluation.

Keywords: Memristor Ratioed Logic, Low Power Design, Encoder, Combinational Logic Circuits, Memristor.

1. INTRODUCTION

The relentless pace of technological advancement, as epitomized by Moore's law, has fueled the continuous expansion of transistor density on semiconductor chips. However, the physical limitations of transistors, coupled with concerns regarding energy consumption and economic viability, pose formidable challenges to sustaining this exponential growth. To perpetuate Moore's law, innovative solutions are imperative, among which lies the exploration of alternative components to traditional transistors [1].

The demand for smaller semiconductor footprints and heightened efficiency in complementary metal-

oxide-semiconductor (CMOS) techniques persists unabated, driving relentless efforts towards innovation. Yet, the downsizing of CMOS cells exacerbates leakage currents, leading to escalated static power dissipation and heightened manufacturing complexity, manifested in increased error rates.

In this pursuit of efficiency and miniaturization, the advent of the memristor emerges as a promising panacea. Coined by Professor Chua in 1971 and materialized by HP Labs in 2008, the memristor has garnered attention for its potential across a spectrum of applications, from field-programmable gate arrays (FPGAs) to amplifiers [2]. Memristors offer a pathway to circumvent the limitations posed by conventional transistors, promising advancements in manufacturing simplicity and addressing area constraints [3].

However, not all memristor-based logic paradigms are created equal. While memristor-aided logic (MAGIC) and material implication (IMPLY) memristor logics have been proposed, their efficacy is marred by inconsistencies in multiple fan-outs and complexity. Nonetheless, memristors find compelling utility in diverse domains, including memory, neuromorphic systems, and analog circuits.

Of particular interest is the application of memristors in logic circuits, where they serve as fundamental building blocks for innovative designs. In this digital realm, the manipulation of memristance delineates logic states, with high memristance representing logic 0 and low memristance signifying logic 1 [3].

Within this context, the encoder emerges as a pivotal circuit in digital systems, facilitating signal encoding and streamlining data selection processes. Leveraging memristor ratioed logic (MRL), this work endeavors to pioneer a novel approach to encoder design, prioritizing power efficiency and comparing favorably against incumbent CMOS and pseudo-NMOS circuit logics.

Need for Encoders : In the realm of digital logic, encoders assume paramount importance, serving as linchpins in information processing and data communication. Encoders compress data, reduce redundancy, and streamline data transmission and storage, making them indispensable in various applications.

2. BASICS OF MEMRISTOR

A memristor, a fundamental passive element with two terminals, is characterized by its non-volatile nature and its role as the fourth fundamental circuit element, linking magnetic flux and charge, as depicted in Figure 2.1.

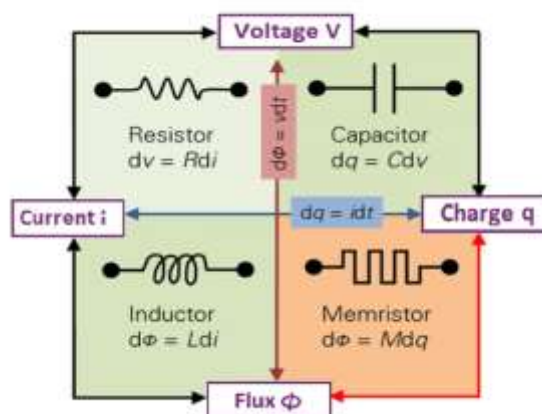


Figure 2.1: 4 - Passive elements

The circuit representation of a memristor symbol is illustrated in Figure 2.2. The relationship between charge (q) and magnetic flux (ϕ) is governed by the equation $M = d\phi/dq$, where M represents memristance measured in ohms, q is – charge (in coulomb) & ϕ is - magnetic flux (in Volt-second).

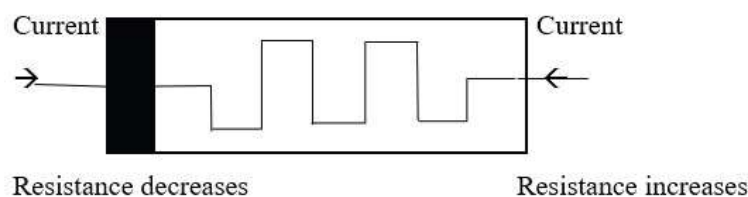


Figure 2.2: Memristor model

Constructed between two platinum metal layers, the memristor comprises pure (undoped) titanium dioxide (TiO_2) serving as a dielectric, with doped titanium dioxide (TiO_{2-x}) acting as a semiconductor atop the dielectric. The current flowing through the memristor induces variations in its resistance [4]. The resistance assumes a low value, termed as ON resistance (R_{on}), when the width of the doped region surpasses that of the undoped region of TiO_2 . Conversely, the resistance escalates, reaching a high value known as OFF resistance (R_{off}), when the width of the undoped region exceeds that of the doped region. The polarity of a Memristor is indicated by the black thick line [5]. Typically, the ratio of R_{off} to R_{on} is equal to or greater than 1000.

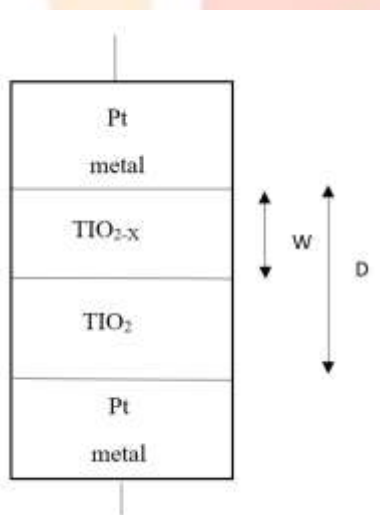


Figure 2.3: Constructional view of Memristor

The variation in resistance of the memristor is mathematically described by the equation:

$$R(w) = R_{on} (w/D) + R_{off} (1 - w/D)$$

In this equation, w represents the width of the doped TiO_2 , and D signifies the total width of the TiO_2 layer. The width of the undoped region of the memristor is influenced by the magnitude of the supply current, resulting in either overshoot or undershoot, as depicted in Figure 2.4 [6].

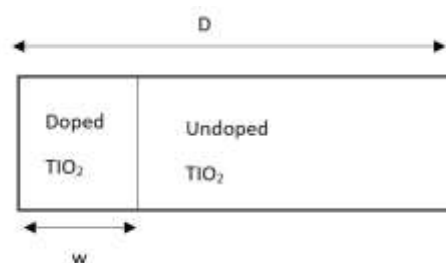


Figure 2.4: Simple representation of Memristor

A. Memristor Ratioed Logic

Memristor Ratioed Logic (MRL) represents a hybrid approach to logic gate design, leveraging both CMOS technology and memristors. This innovative paradigm offers several advantages over conventional CMOS designs [7]:

I. Fabricating memristors atop the CMOS poly-silicon layer simplifies the manufacturing process and reduces design area.

II. MRL reduces the number of transistors required for logic gate implementation [8], contributing to circuit simplification and efficiency.

III. Signal attenuation in MRL is notably lower compared to other memristor-based logic paradigms such as MAGIC and IMPLY logic [10] [11].

Figure 2.5 illustrates the construction of a NAND gate using two memristors (M1 and M2) connected in parallel, with the output fed into a CMOS inverter. When both inputs (A and B) are set to 0, resulting in zero potential across the terminals, the output of the CMOS inverter is asserted to 1 [9].

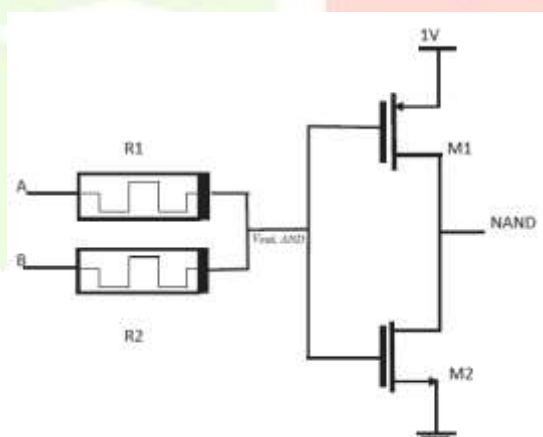


Figure 2.5: NAND gate using Memristor

Similarly, as depicted in Figure 2.6, a NOR gate logic configuration is achieved by reversing the polarity terminals of the memristors in the architecture described in Figure 2.5.

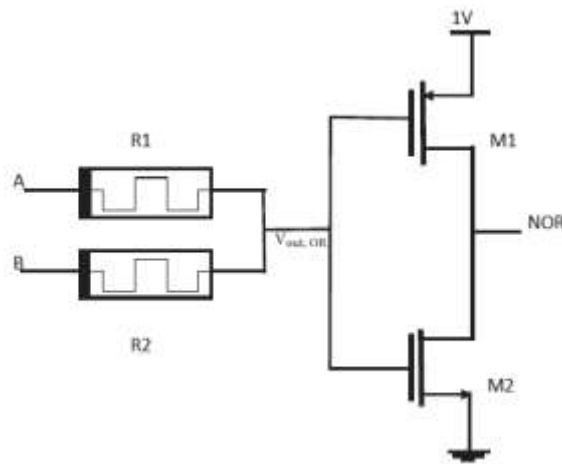


Figure 2.6: NOR gate using Memristor

B. Memristor Model & Window Function

In this paper, the encoder circuit is modeled utilizing the Linear Ion Drift Model of memristors. The Linear Ion Drift Model is characterized by the following equation:

$$R(w) = R_{on} (w/D) + R_{off} (1 - w/D)$$

This model assumes a linear relationship between the width of the doped region and the input current, described by the equation:

$$dw/dt = (uv R_{on}) / Di(t)$$

The model offers simplicity and ease of implementation, featuring symmetry and leveraging the window function defined as:

$$F(w) = 1 - (2w/(D-1))^{2p}$$

In the context of memristor modeling, it's crucial to address the possibility of the memristor width overshooting physical dimensions. To mitigate this issue, window functions are employed during simulation to confine the width within the physical boundaries of the memristor. Various models of window functions, such as Biolek and Joglekar, are available for this purpose [10] [12]. This paper adopts a modeling approach for the encoder circuit that incorporates the Ion Drift Model in conjunction with the Joglekar window function of memristors. By leveraging this combined methodology, the encoder design ensures accurate simulation results while adhering to the physical constraints of memristor dimensions.

3. ENCODER DESIGN & OPERATION

In digital logic circuits, encoding information into binary bits with specific meanings is a fundamental operation. Facilitating this process is the encoder circuit, designed to perform the encoding function efficiently. When one of the input bits reaches an effective level, the encoder responds by changing its output in accordance with the input bits. Typically, an encoder circuit consists of 'N' outputs and 'M' inputs, with the relationship between them defined by $M = 2^N$.

Illustrated in Figure 3.1, the encoder diagram provides a visual representation of the circuit's structure and connectivity. Table 3.1 complements this by presenting the truth table, outlining the correspondence

between input combinations and the resultant encoded outputs.

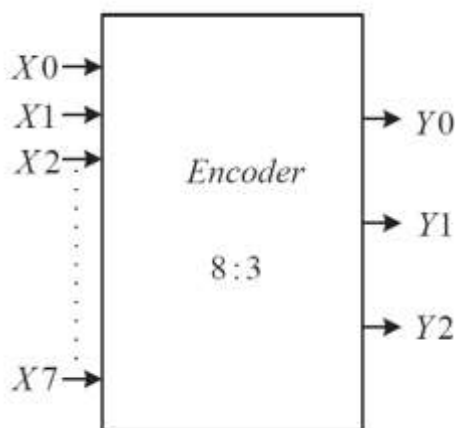


Figure 3.1: 3 Bit Encoder

X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Table 3.1: 3 Bit Encoder Truth Table

The relationships between the encoder's inputs and outputs, as delineated in the truth table, provide valuable insights into the encoding process:

$$Y_0 = X_1 + X_3 + X_5 + X_7$$

$$Y_1 = X_2 + X_3 + X_6 + X_7$$

$$Y_2 = X_4 + X_5 + X_6 + X_7$$

These relations lay the groundwork for implementing the logic circuit using various methodologies, including CMOS, Pseudo NMOS, and MRL.

3. 1 ENCODER DESIGN USING MRL

Tool Used: LTspice (180nm Technology)

Memristor Specifications: $R_{on}=1\Omega$, $R_{off}=10M\Omega$ and initial resistance $R_{init} = 8M\Omega$

As shown in the figure 3.2, In order to realize output function Y_0 - transistors M1-M4 forms the pull down network and memristor acts as a pull up network. That is 4 transistors and 1 memristor constitute a 4 input NOR gate. X_1 , X_3 , X_5 & X_7 are the input signals that pass through the NOR gate and the signal at the drain of M1 is inverted signal of $(X_1 + X_3 + X_5 + X_7)$. Here, M5 and Memristor constitute an inverter. The output of 4-input NOR gate is given as the input of inverter. The signal at the drain of M5 is $Y_0 =$

$X1+X3+X5+X7$. Similarly, a combination of 4-input NOR gate and an inverter has been used for each output of 3-bit encoder [13].

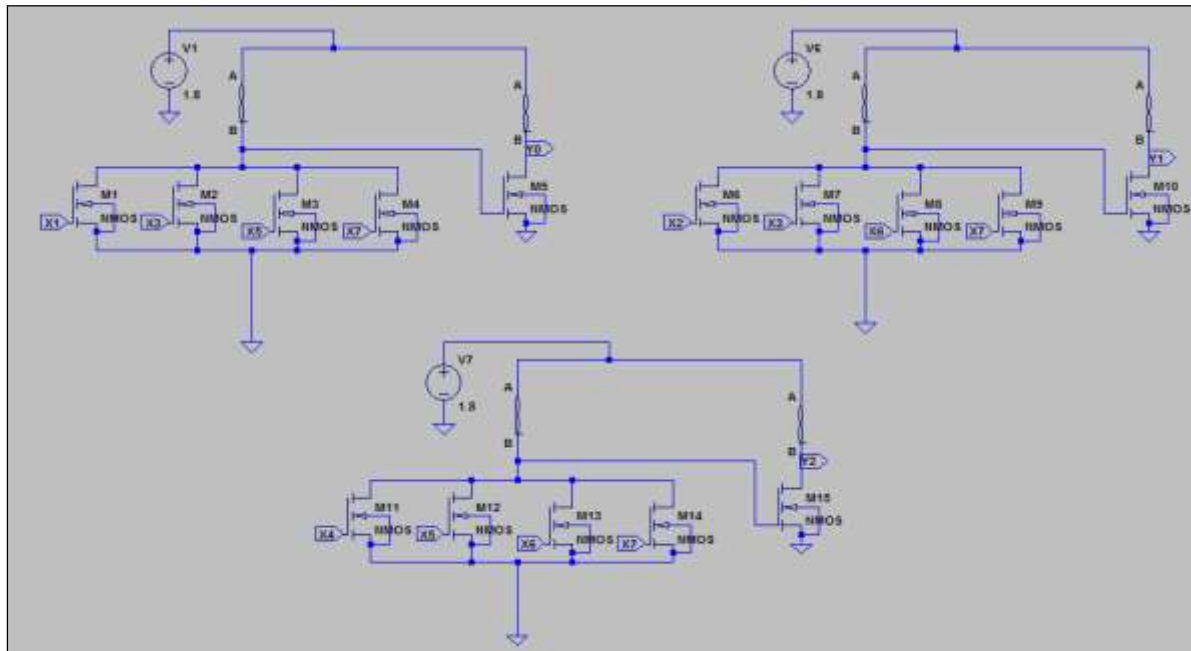


Figure 3.2: 3 Bit Encoder using MRL

3.2 ENCODER DESIGN USING CMOS LOGIC

In this implementation, 4 NMOS transistors forms the pull down network and 4 PMOS transistors from the pull up network to realize a NOR gate and its output is fed to a CMOS inverter to implement the encoder output expressions.

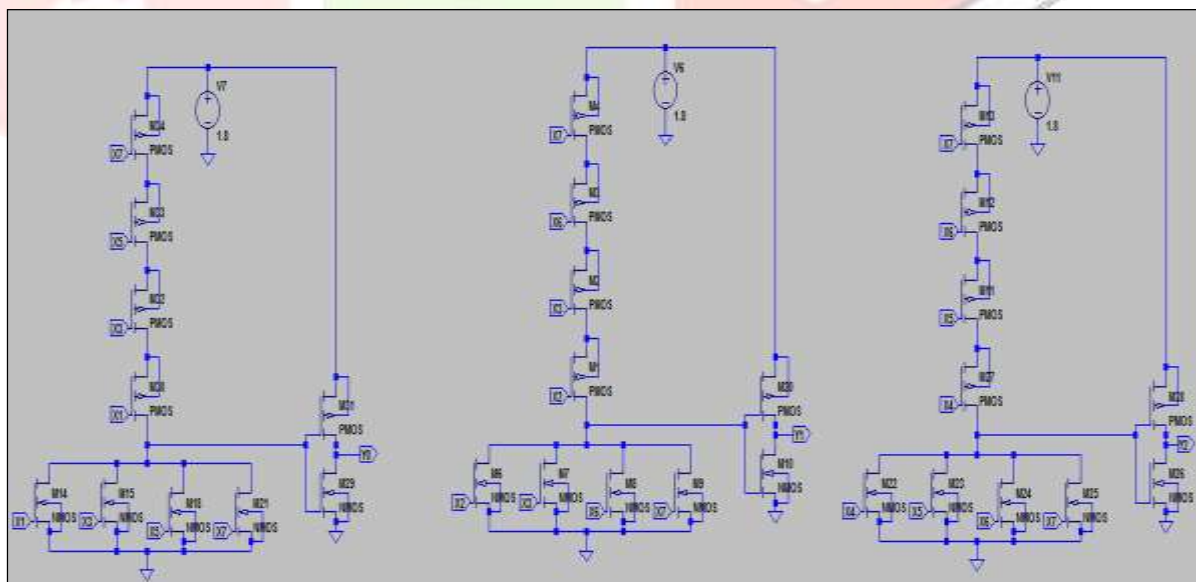


Figure 3.3: 3 Bit Encoder using CMOS Logic

3.3 ENCODER DESIGN USING PSEUDO NMOS LOGIC

In this implementation, 4 NMOS transistors forms the pull down network and 1 PMOS transistors from the pull up network to realize a NOR gate and its output is fed to a pseudo NMOS inverter to implement the encoder output expressions.

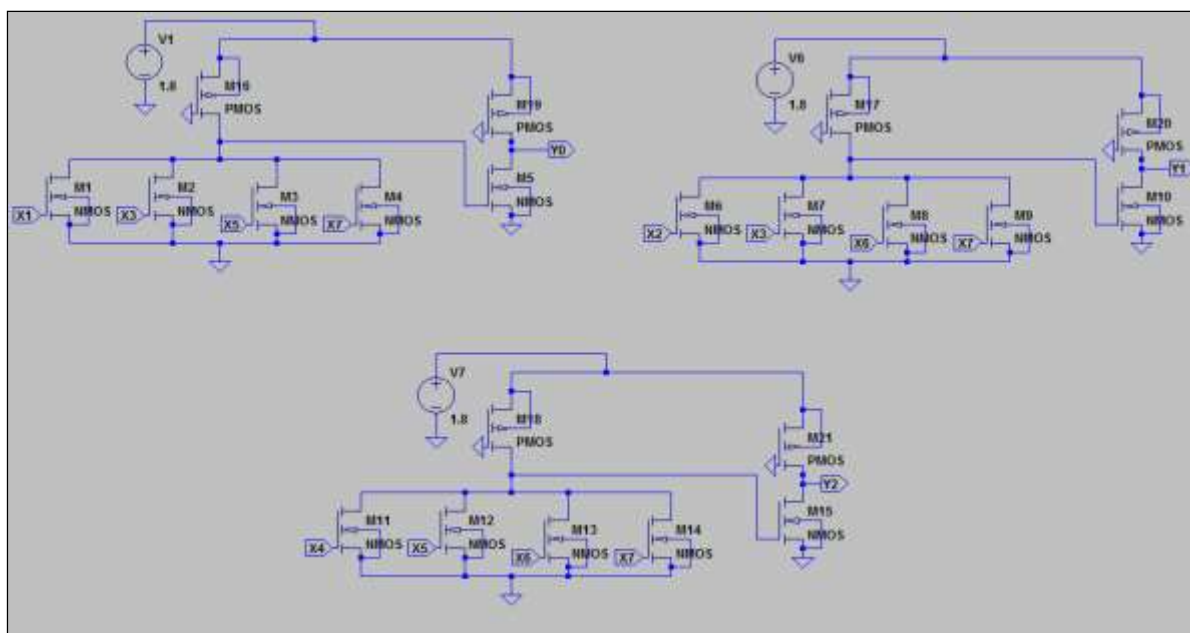


Figure 3.4: 3 Bit Encoder using Pseudo NMOS logic

4. RESULTS AND DISCUSSION

Figure 4.1, is the simulation output of 3 Bit encoder output using Memristor Ratioed Logic which is same as the truth table of encoder.

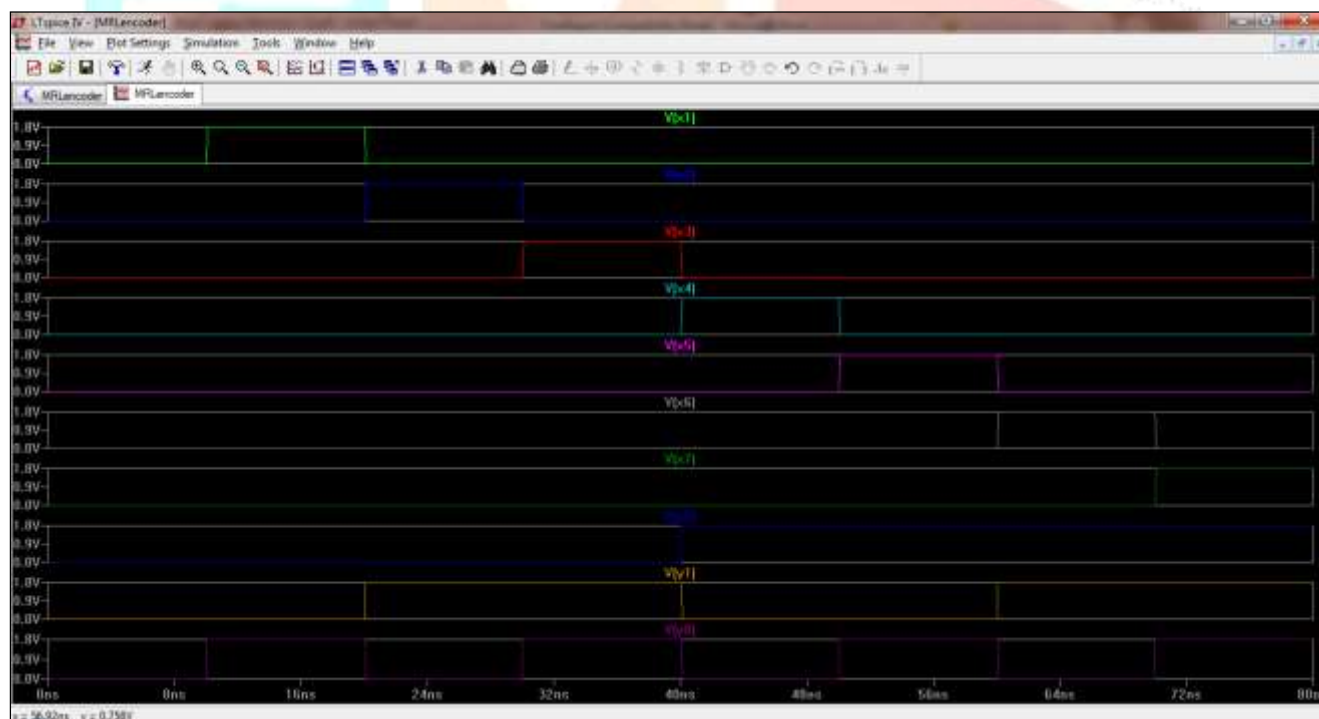


Figure 4.1: Output of Encoder using MRL

Figure 4.2, shows the power analysis of 3 Bit encoder output using Memristor Ratioed Logic and the average power dissipated during the analysis is found to be **1.2149 μ W**.

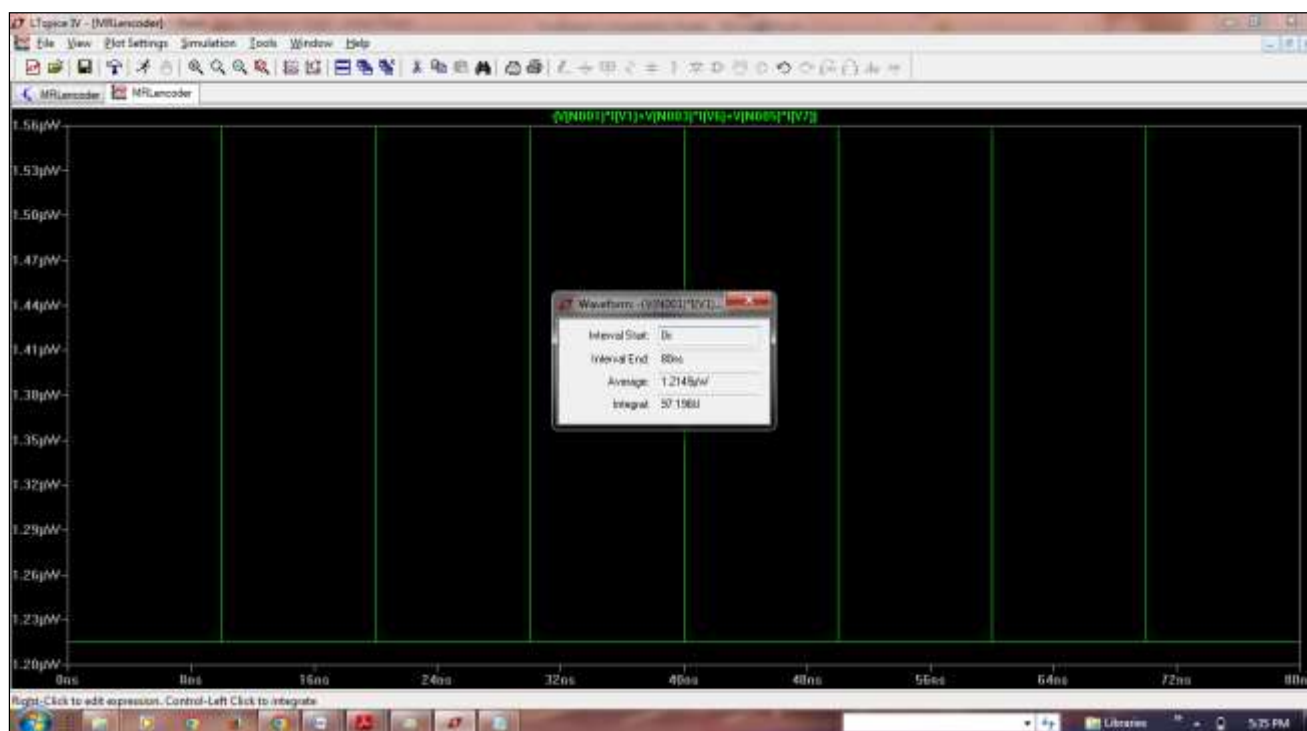


Figure 4.2: Power analysis of Encoder using MRL

Figure 4.3, is the simulation output of 3 Bit encoder output using CMOS Logic which is same as the truth table of encoder.

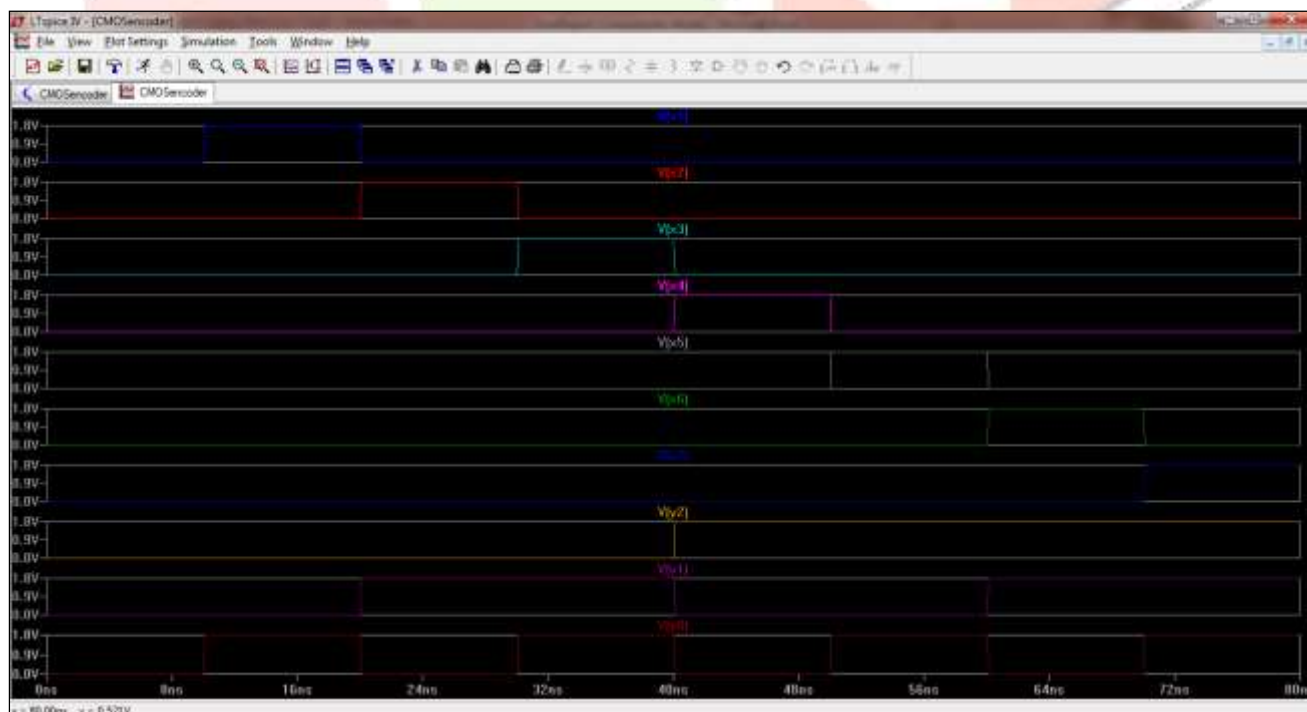


Figure 4.3: Output of Encoder using CMOS Logic

Figure 4.4, shows the power analysis of 3 Bit encoder output using CMOS Logic and the average power dissipated during the analysis is found to be **1.5101 μ W**.

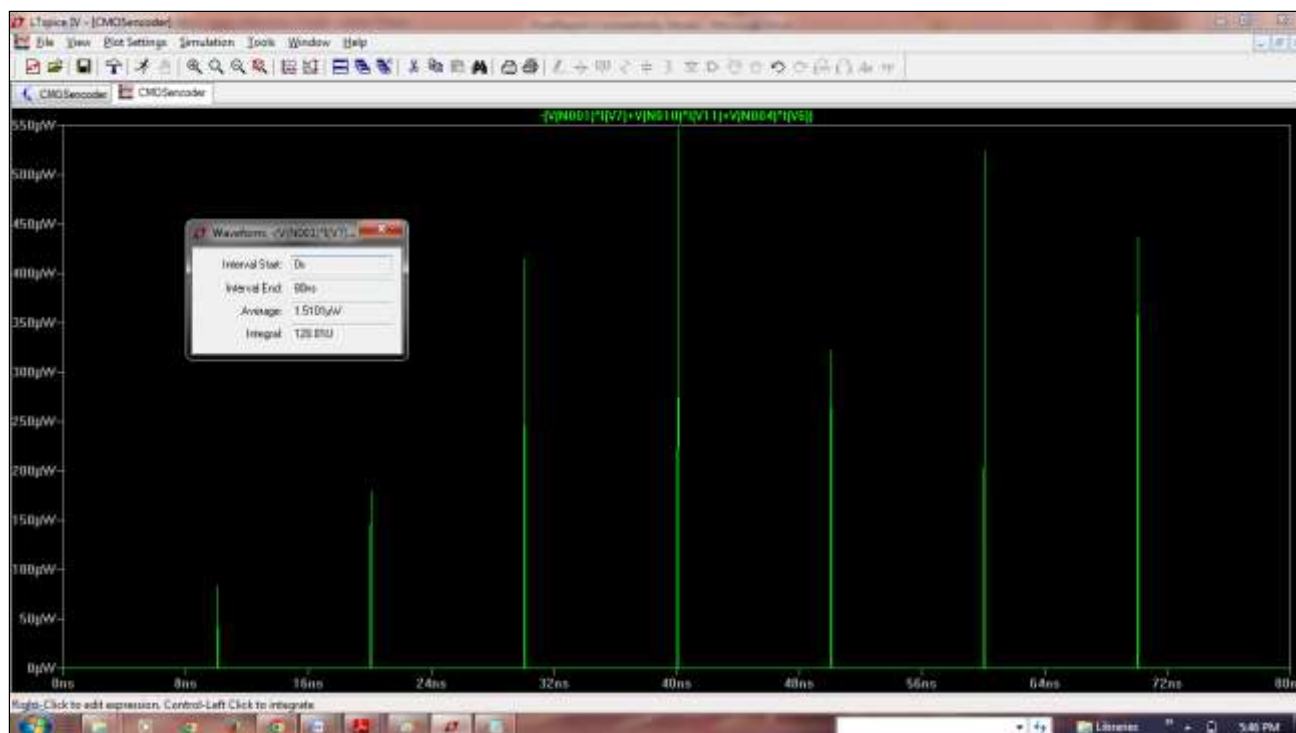


Figure 4.4: Power analysis of Encoder using CMOS logic

Figure 4.5, is the simulation output of 3 Bit encoder output using Pseudo NMOS Logic which is same as the truth table of encoder.



Figure 4.5: Output of Encoder using Pseudo NMOS Logic

Figure 4.6, shows the power analysis of 3 Bit encoder output using Pseudo NMOS Logic and the average power dissipated during the analysis is found to be **176.11μW**.

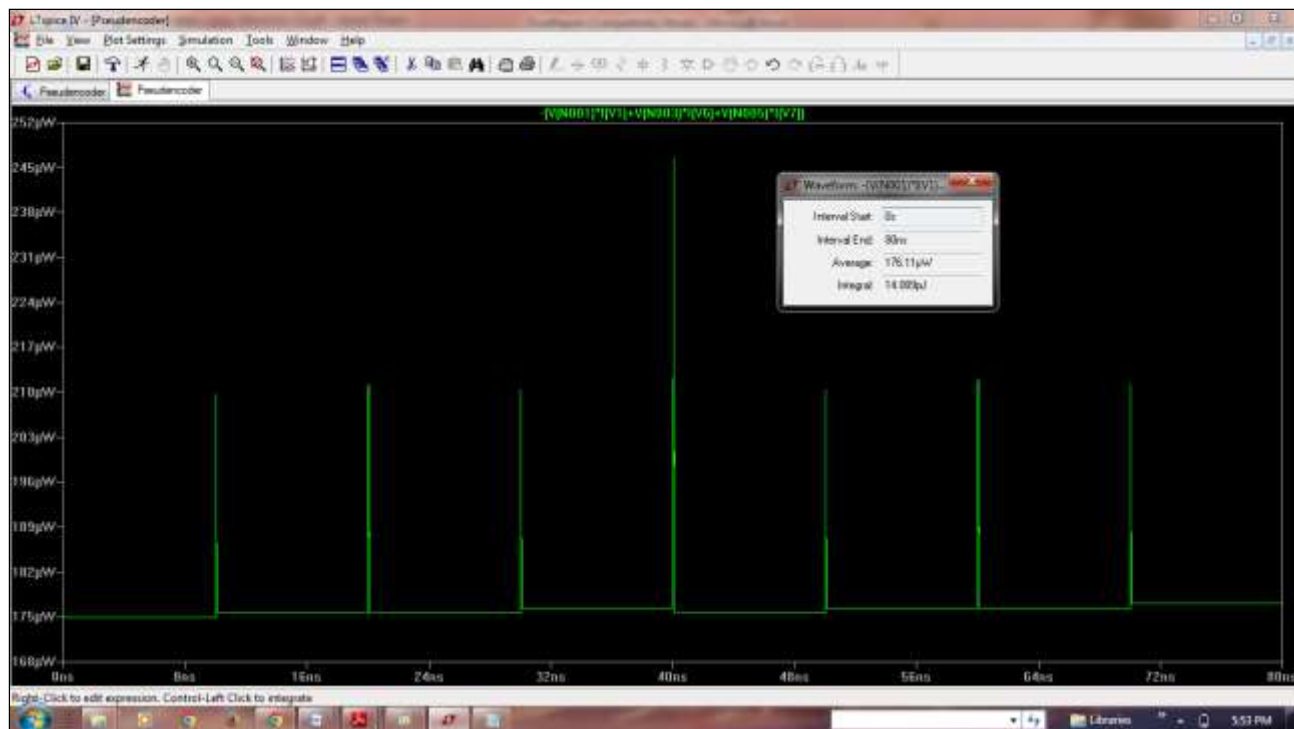


Figure 4.6: Power analysis of Encoder using Pseudo NMOS logic

Comparison:

It is seen that the power dissipation of the Encoder circuit using the MRL is less than the CMOS logic and very less as compared to the Pseudo NMOS logic.

3 Bit Encoder Design Using:	Average Power Dissipation (180nm technology)	Number of Components
Memristor Ratioed Logic	1.2149µW	21 Components (6 Memristors and 15 NMOS)
CMOS Logic	1.5101µW	30 Transistors (15 PMOS and 15 NMOS)
Psuedo NMOS Logic	176.11µW	21 Transistors (6 PMOS and 15 NMOS)

Table 4.1: Comparison of Results

Since the area occupied by a Memristor based design is lesser than CMOS, it can be depicted that this design is efficient with respect to the area consumed [11], [14], [15]. It can be seen that the number of transistors that are required for this design is the least when compared to the conventional CMOS and Pseudo NMOS logic. By using CMOS technology, the encoder circuit has 30 transistors, of which 15 PMOS and 15 NMOS. By using Pseudo NMOS technology, the encoder circuit has 21 transistors, of which 6 PMOS and 15 NMOS. By using MRL technology, the encoder has 21 elements, of which 6 Memristors and 15 NMOS.

5. CONCLUSION

The implementation of an encoder using Memristor-based logic design proves significantly superior in terms of power efficiency and area utilization compared to traditional CMOS logic and Pseudo NMOS logic. While the trade-off between power, area, and speed remains a persistent consideration in circuit design, our findings underscore the remarkable advantages of this approach. By significantly reducing the transistor count required, this design technique not only enhances efficiency but also presents a more streamlined and effective method for digital circuit design. As such, the adoption of Memristor-based logic holds immense promise for advancing the development of next-generation digital systems.

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