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DESIGN OF BANDGAP VOLTAGE REFERENCE CIRCUIT WITH LOW TC AND HIGH PSRR IN 180nm CMOS TECHNOLOGY

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Abstract: In this paper a low power, high precision bandgap reference is proposed and analyzed. The voltage reference is obtained by summing a proportional-to-absolute-temperature (PTAT) voltage and a complementary-to-absolute-temperature (CTAT) voltage. In this paper CTAT voltage is obtained from conventional circuit i.e.; based on a scaled emitter-base voltage of a BJT and PTAT voltage is obtained by using current mirror structure and as well as by using operational amplifier. The designed circuit was implemented using Cadence Virtuoso in CMOS 180nm process technology. A new low temperature coefficient (TC) high power supply rejection ratio (PSRR) bandgap voltage reference is presented in CMOS technology. In order to achieve low TC and high PSRR voltage reference with small area overhead and good practicability, the proposed circuit uses a curvature correction method based on sub-threshold current and a PSRR enhancement circuit. When the power supply voltage is 1.8V, this circuit is devised and verified using 0.18um CMOS process. The results show the output voltage is constant at 1.2V at room temperature. The TC is 6.1ppm/°C in a wide temperature range of -40°C to 125°C. The measured PSRR is -70dB.

Keywords: CTAT, PTAT, TC, PSRR

I. INTRODUCTION

In these modern days, the Integrated Circuits are being designed to achieve higher integration and higher performance. While in modern electronics, digital technology has got to be the development trend, a part from this, analog circuits still play an incomparable role. The signals generated by most electronic devices are analog. These signals must be processed before digital processing and after digital processing; the signal must be converted into analog at the output. The research on analog IC design using CMOS technology becomes very important since the CMOS technology has been widely used. I proposed to design a very efficient bandgap reference. Bandgap reference circuit is a circuit designed to produce a stable and precise output reference voltage which is independent of variations in Process, Temperature and Voltage.

II. INTRODUCTION TO CADENCE

The software tool used to construct the bandgap reference circuit is cadence virtuoso. The Cadence virtuoso system platform design is a holistic, system-based solution and it provides the functionality to drive simulation and LVS-clean layout of integrated circuits and packages from single schematic. There are two main functionalities of cadence virtuoso, they are implementation and analysis.

The implementation flow is used to create an Integrated circuit package schematic in virtuoso schematic editor and it transfer the whole schematic data to cadence Sip layout to layout the physical design. In addition, this flow offers the capability to generate and verify library parts, output a bill of materials (BOM), and perform layout versus schematic (LVS) checking.

III. BLOCK DIAGRAM

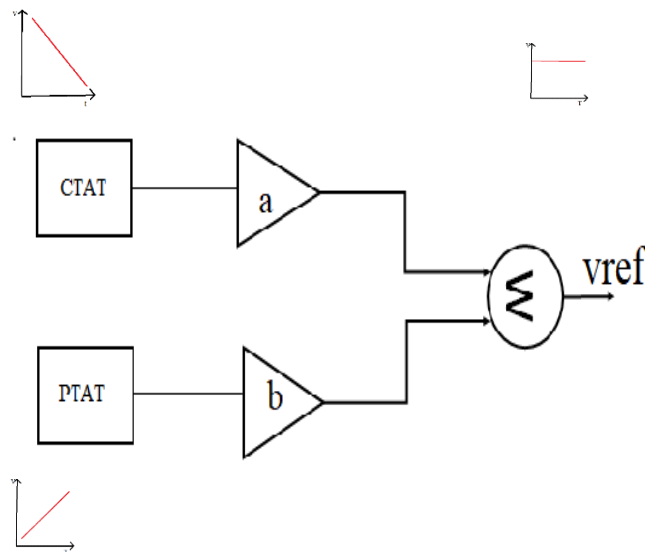


Figure.1 Block diagram of BGR circuit

IV. DESIGN OF CTAT

The CTAT is traditionally generated from a diode (or) diode-connected BJT. The diode voltage drop across the base-emitter junction, V_{BE} of a BJT changes complementary to absolute temperature (CTAT). The I-V relationship for a bipolar junction transistor can be

$$V. \quad I_C = I_S e^{\frac{V_{BE}}{N V_T}}$$

where V_{BE} is the base-emitter voltage of a diode or a diode-connected bipolar transistor, I_C is the collector current, I_S is the saturation current, N is the non-ideality factor and V_T is the thermal voltage. The above equation can be rearranged as

$$VI. \quad V_{BE} = N V_T \ln\left(\frac{I_C}{I_S}\right),$$

Where the current I_S which is CTAT in nature, more dominant than threshold voltage. Hence, the resultant voltage becomes CTAT. Figure2 illustrates the implementation of CTAT circuit with experimental results in which the CTAT voltage decreases with a range of slope of -1.7 to -2.05mV/°C.

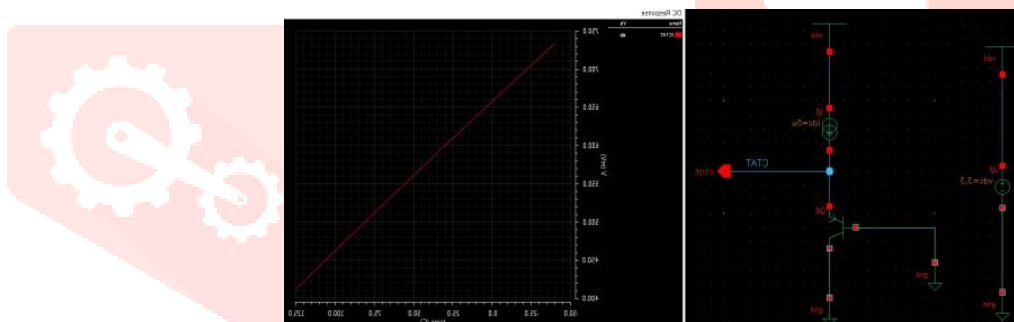


Fig. 2. CTAT circuit with experimental results

III. DESIGN OF PTAT

When two BJTs are operated with unequal current densities and areas, then the difference in the base-emitter voltages, ΔV_{BE} of the transistors is proportional to absolute temperature (PTAT). The PTAT is given as

$$V_{BE} = V_T \ln(n)$$

Where, $\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln(n)$ and $V_T = kT/q$

Where k is Boltzmann's constant, T is the absolute temperature; q is the electron charge, of the two BJTs, respectively.

In above equation, the voltage difference in the base emitter voltages of transistors is directly proportional to the threshold voltage, i.e. directly proportional to the temperature. The experimental results of PTAT are illustrated in Figure 3 and figure 4.

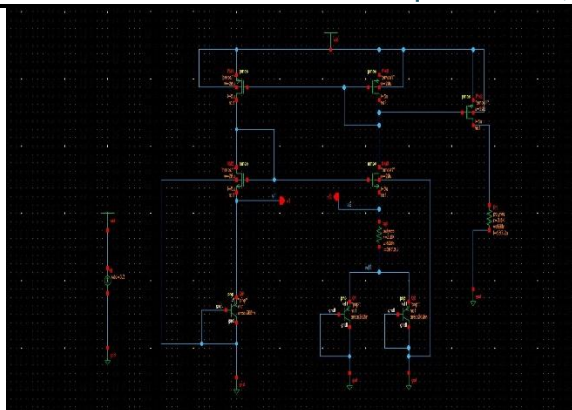


Figure 3. PTAT circuit

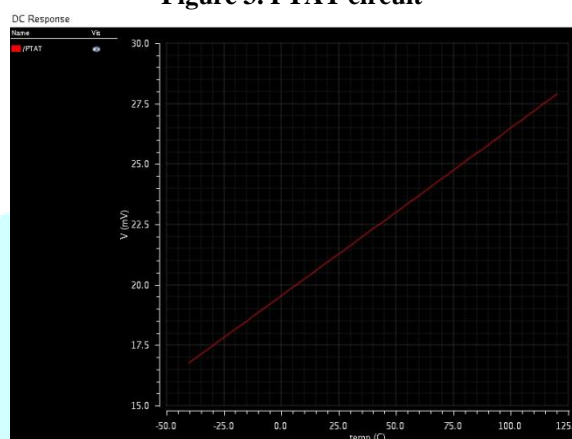


Figure 4. Experimental results of PTAT

IV. DESIGN OF BANDGAP REFERENCE

BGR circuit is combinational of CTAT circuit and PTAT circuit. The output voltage of this circuit is constant with respect to temperature. This BGR circuit produces a constant output voltage with respect to change temperature, pressure. A bandgap core circuit and a start-up circuit are included in this approach. The bandgap core is a PTAT circuit which will be proportionate to absolute temperature and the output circuit acts as a CTAT circuit which means compliment to absolute temperature. The OP-Amp used in this circuit will provide high gain. The circuit diagram of this conventional BGR.

BGR circuit with constant voltage and current outputs is presented with a 1.2 V supply voltage. The first stage provides a fixed BGR voltage of 1 V with a temperature coefficient (TC) of 6.1 ppm/ 0 C. It includes a 2-stage op-amp for higher power supply rejection ration (PSRR). The op-amp has a closed feedback loop to neglect the current proportional-to-absolute-temperature (PTAT) and the negative TC. The second stage provides a higher current gain and an enhanced PSRR. It produces a fixed BGR current of 100 μ A. Simulation results including PVT variations and Monte Carlo analysis have been performed, in 180 nm CMOS technology, to the proposed design which achieves a chip area of 0.03 mm², a higher temperature range of -40~125 0 C, a 35 ppm/ 0 C TC, a -70 dB PSRR .

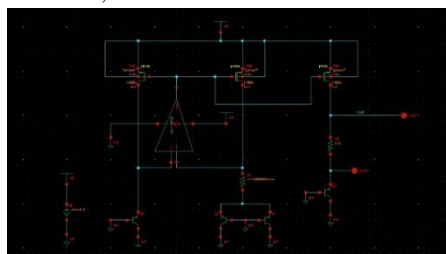


Figure.5 Proposed bandgap reference circuit

This circuit is designed and simulated by using cadence virtuoso. The experimental results are illustrated in Figure.6.

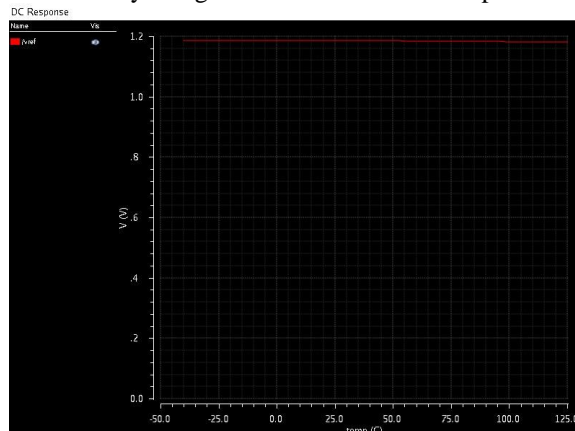


Figure 6. Experimental results of proposed BGR.

VII. CONCLUSION

Based on the standard 0.18nm CMOS technology devised a low TC and high PSRR bandgap voltage reference in this review. The circuit shows great in general execution by performing the temperature characteristic at high temperature and adding PSRR to enhance the circuit. The improved BGR proposed in this paper have the benefits of low power utilization, little region and basic devise technique, circuit is reasonable for all CMOS technology. From the simulation results, the temperature coefficient is simply 6.1 ppm/°C in the scope of - 40°C to 125°C, the low-frequency power supply rejection proportion is – 70 dB.

	This design	[1]	[2]	[3]
Process	0.18μm CMOS	0.5μmBiCMOS	0.35μm CMOS	0.13μm CMOS
Temperature	-40 to 125	-40 to 125	-15 to 150	-55 to 125
Supply	1.8	5	2.5	1.2
Reference voltage(V)	1.2	1.264	0.6177	0.3
TC (ppm/°C)	6.1	8.9	3.9	65
PSRR (dB)	-70	-73		-109

Table-1 Performance comparison

VIII. REFERENCES

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