IJCRT.ORG ISSN : 2320-2882
INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)
An International Open Access, Peer-reviewed, Refereed Journal

HARMONICS MITIGATION IN THREE PHASE ADJUSTABLE SPEED DRIVE USING H-INFINITY CONTROLLER

*T. Chandra Sekar[1],P.Paramasivan[2], A.Kannan[3], B. Justus Rabi,[4]
[1] Associate Professor, Christian College of Engineering and Technology,
Department of EEE, Oddanchatram, Tamil Nadu, India.
[2]Assistant Professor, Christian College of Engineering and Technology,
Department of EEE, Oddanchatram, Tamil Nadu, India.
[3] Professor, Dr.MGR Educational and Research Institute,Maduravoyal, Chennai, Tamil Nadu
[4]Professor, Christian College of Engineering and Technology, Oddanchatram, Tamil Nadu, India

ABSTRACT

This paper describes a novel approach to improve the power factor (PF) and reduce the harmonics generated by an adjustable-speed drive (ASD) using H-Infinity controller and feasible test is conducted to verify the experimental results. A High-Frequency current injection technique is used to improve the harmonic performance and PF. The High Frequency current at the same switching frequency is injected in the input of a front-end rectifier from the output of an HF inverter. All the switches are operated at zero-voltage switching. The diodes of the rectifier are also operated with soft switching at both turn-on and turn-off. Varying switching frequency with a fixed duty ratio regulates the output voltage. The main feature of this circuit is that it does not require any additional active devices for current injection. The inverter driving the IM is operated using an H-infinity sinusoidal pulse width-modulation technique. The circuit simulation results for 0.5-hp induction motor is presented.

Key words: **Adjustable speed drive, High frequency, H-Infinity controller, Power factor, Total harmonic distortion, Zero voltage switching.**

1.INTRODUCTION

Power converters are mainly used in industrial applications due to the unforgettable progress made in the high power electronic devices. In most of the AC-to-DC power converters, PWM voltage source inverters supplied from a smooth DC link voltage is preferred. Most electronic equipment's are energized with 50 Hz utility power in which 50% is processed through some power converters. These power converters use common and conventional diode bridge rectifier followed by a DC capacitor. Since these power converters consume energy from the supply only when the line voltage is higher than the DC voltage, the input line current contains more harmonics which affect the power system and interfere with other electronics equipment's. So, these converters have a low power factor of 0.65. International concerns of power quality problems and pollution have brought the use of Power Factor Correction (PFC) converters to feed Induction motor which is used in number of low power applications because of its high efficiency and wide range of speed and harmonic spectra. The filters composed of capacitors and inductors have been used for reducing current harmonics and improving the system power factor. These filters are expensive, huge and sensitive to the supply frequency. The scheme of High Frequency current injection, proposed in is having a high component count and switch stress is high as they have to carry load current as well as HF injection current. In this paper, the converter which comprises of an Active Power Factor Correction Circuit and HF front-end three-phase diode rectifier is proposed. This paper presents the high-power-factor operation of AC-to-DC converter. The high-power-factor is obtained by injecting high-frequency current, at the input of the front-end three-phase rectifier from the HF inverter. All the switches of the inverter shows zero voltage switching. The converter is operating in continuous conduction mode and uses a current multiplier approach with average current control. A high-power-factor is achieved by injecting high frequency triangular current from the output of the three-phase inverter. The HF current at the same switching frequency is injected into the input of a front-end rectifier from the output of an HF inverter. The main advantage of the circuit is that it does not require any additional active devices for current injection. The inverter driving the induction motor is operated using a SPWM technique. These converter topologies can be of potential interest for future work in this area. However they have lower switching losses, the additional control circuitry is required for their operation. The brief modeling and performance analysis is presented in this paper.

2. PROPOSED TOPOLOGY

Harmonics present in the system are reduced by using capacitors and inductor which improves the power factor of the system. The system is built with reduced switching components. The simplified functional block diagram and circuit diagram of the proposed scheme are shown in below. It consists of a 3-phase diode bridge rectifier with source inductors. A dc-link capacitance and a three-phase full-bridge inverter. It has a ripple current at the switching frequency therefore; the input dc source impedance seen by the inverter is small. Hence, a small value of the dc-link capacitance suffices.

3. BLOCK DIAGRAM

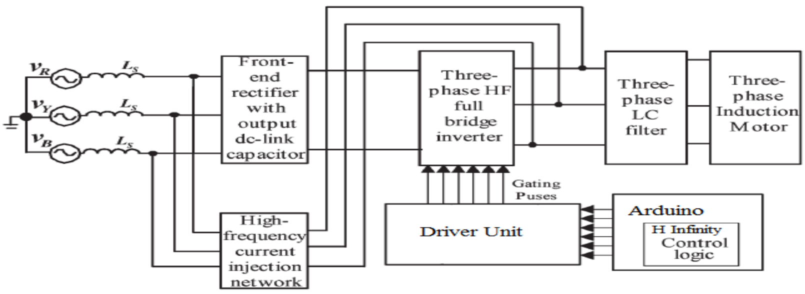

Fig.1 block diagram of an ASD

The HF inverter output is fed to the 3-phase induction motor through small LC filters. The HF current from the inverter output is also feed back to the input of the diode bridge rectifier through an HF current injection network. The current injection network consists of three sets of inductor Lf and capacitor Cf. The inverter is operated using a sinusoidal PWM (SPWM) technique with a reference frequency of 50 Hz and a carrier frequency of 33 kHz. Thus, the HF current at 33 kHz is injected into the input of a front end rectifier from the output of an HF inverter. The SPWM switching signals are generated using H-Infinity controller. The inverter switches maintain zero-voltage switching (ZVS) for considerable period of the output phase voltage. Zero Voltage Switching is not maintained only at the peak of output voltage. The SPWM technique provides a maximum duty ratio, because of peak of the output phase voltage i.e., the "on" time period of the switch is longer when compared with the "off" time period. This off time period is not enough for the inverter output current to reset to zero. So, an anti parallel diode of the device does not conduct before the conduction of the main switch, as the main switch continually conducting in the next switching cycle. Thus, the turn-on losses are reduced to a significant level, but they are not completely eliminated. Then on-ZVS period is eliminated by keeping a small modulation index and a maximum duty ratio of about 0.5. The turn-off losses are reduced by connecting a snubber capacitor Cn across each switch.

4. PRINCIPLE OF OPERATION

The ac input line current of the 3-phase diode bridge rectifier has a discontinuity in periods 0◦ to 30◦, 150◦ to 210◦, and 330◦ to 360◦ in one cycle . This is because none of the diodes is forward biased in these periods. It is evident that the diode leg current the resultant sum of the line current i_A and the injected currentiLf1. HF current injection modulates the diode leg voltage v_A- at the injected frequency of 33 kHz. Therefore, the diode bridge rectifier operates at a high frequency. When $irect_A$ is positive, the upper diode D1 conducts, and when $irect_A$ is negative, the lower diode D4 conducts. The modulated voltage provides a sufficient forward bias to the diodes during the valley period. Every diode turns on and turns off at the switching frequency and conducts a complete 180◦ period of the input voltage in the discontinuous mode. When none of the diodes on a leg of the input diode bridge rectifier is in conduction, the input ac line current through that phase is equal to the injected current. It can be seen that the front-end rectifier of the converter operation is similar to that of the three-phase PWM boost rectifier operating with continuous input currents.

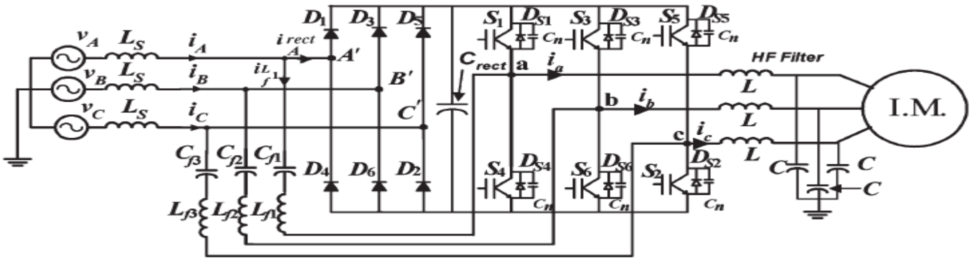

Fig.2 Circuit Diagram

The diodes D_1 and D_4 of the input three-phase diode bridge rectifier turn-on and turn off at the rate of the switching frequency during the positive and negative half-cycles of the ac input supply voltage of phase A, respectively. When switch S_1 turns on, the current through diode D_1 linearly increases from 0 to its peak value ID_1p. Similarly, when switch S_4 turns on, the current through D1 linearly decreases from its peak value $I_{D1}p$ to 0. The current i_{D1} becomes zero at the end of the switching cycle. So, the current through the input rectifier is the HF triangular waveform in a sinusoidal envelope of the supply frequency. The current through the switched inductorL_{f1} is also a triangular waveform. It linearly decreases from $+IL_{f1}p$ to $-IL_{f1}p$ during the time interval Ton=dTs and linearly increases from $-IL_{f1}p$ to $+IL_{f1p}$ during the time $T_{off} = (1 - d)Ts$, where d is the duty ratio, and T_{on} and T_{off} are the on and off periods of the switching device of the HF inverter, respectively. The peak value of the rectifier current $I_{D1}p$ is equal to $2IL_{f1p}$. The peak values of the HF injected current and diode current vary over the cycle of the input supply voltage. In the HF current injection network, capacitor C_f provides dc blocking for the HF injected current IL_{f1}. Hence, the current IL_{f1} is an alternating current without any dc offset, whereas the same current that is flowing through the diode is unidirectional. The peak-to-peak value of the HF injected current and the peak value of the current through D1 is the same i.e., $ID1p= 2IL_{f1p}$.

5. SIMULATION OUTPUT

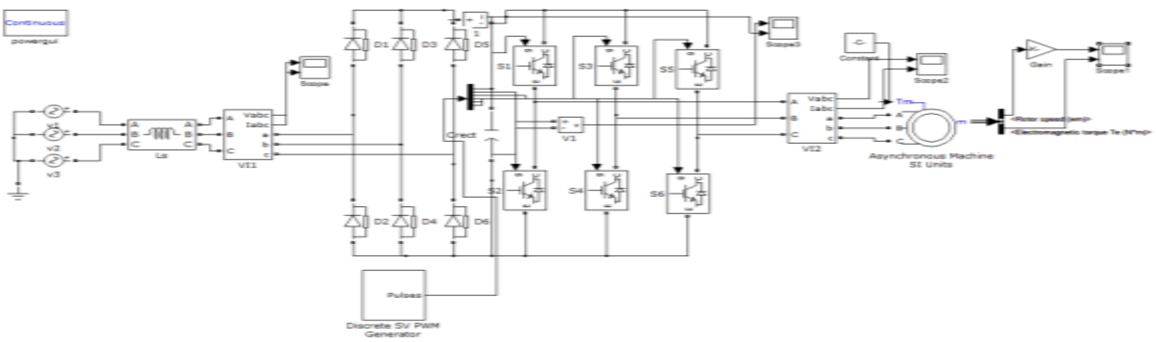

Fig.3 Without current injection

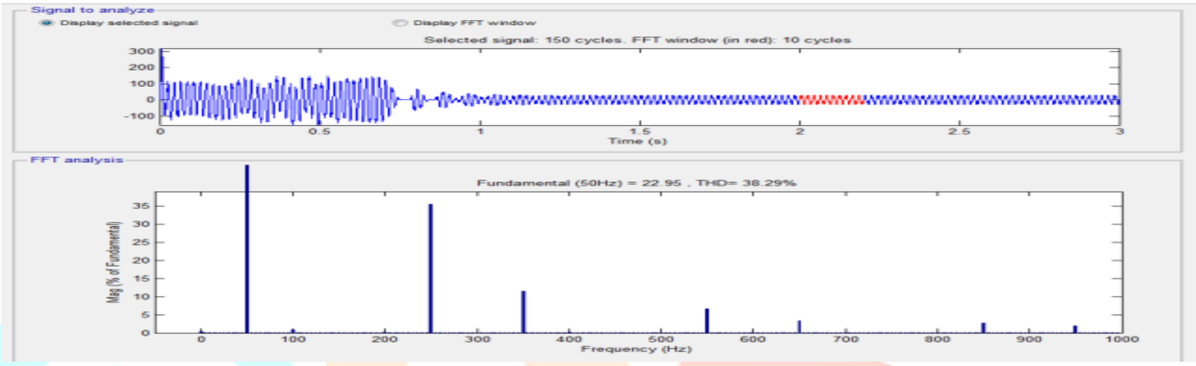

Fig.4 THD for without current injection

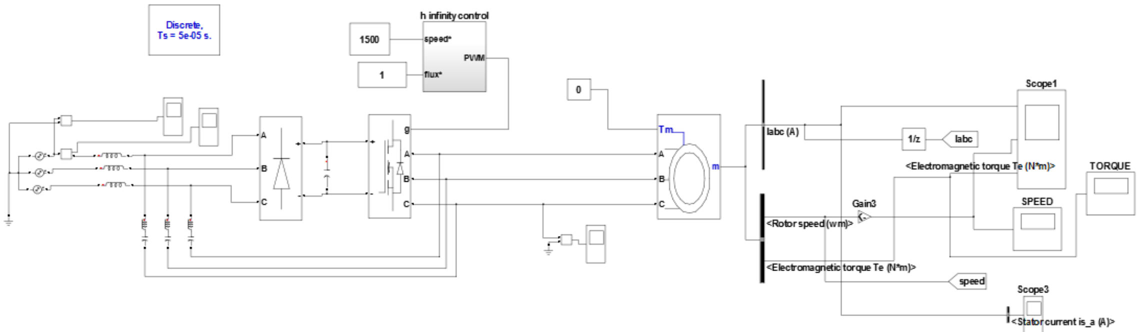

Fig.5.With current injection

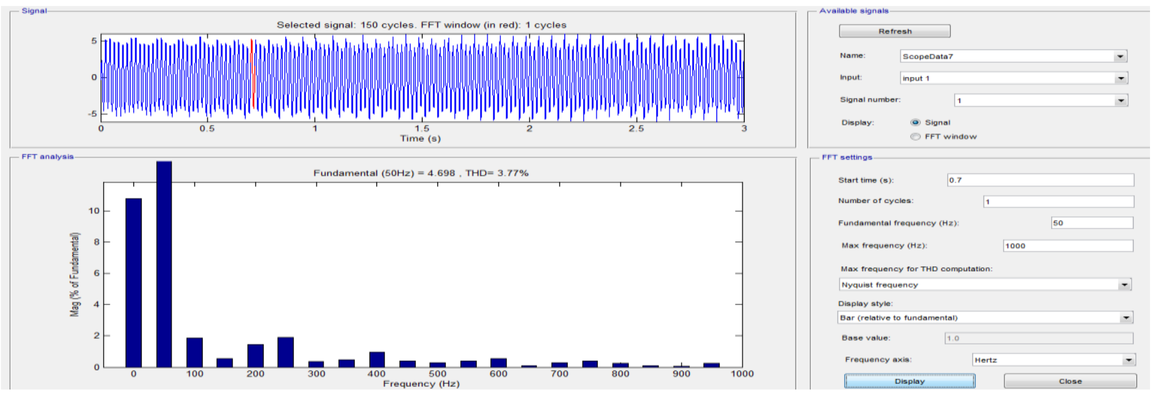

Fig.6 With current injection by FFT analysis

6. CONCLUSION

An ASD with high input PF and improved harmonic performance has been proposed. The PF of the three-phase ac input line current is improved by using HF current injection. The main advantage of this approach is that it does not require any additional active component for HF current injection. Due to the current injection at a high frequency, inductors Lf and capacitors Ci have small values. The inverter switches maintain ZVS for most of the period of the output phase voltage, except at the peak of the output voltage. A maximum duty ratio of about 0.5, By keeping a small modulation index, the non-Zero Voltage Switching period is eliminated. To study the performance of the proposed technique on a high-power drive, the converter feeding a 0.373-kW induction motor has been simulated using MATLAB SIMULINK. Detailed experimental results of the proposed scheme for a 0.5-hp induction motor have also been given to verify the performance of the proposed scheme. It is observed that the high PF is maintained under different loading condition

REFERENCES

[1] *Chandra Sekar, T., B. Justus Rabi and A. Kannan, 2014. "Harmonics Reduction in Front End Rectifier of Uninterruptible Power Supplies with Active Current Injection" –Australian Journal of basic and Applied Sciences, 8(6): 132-137.*

[2] *S. Vijayan, S. Paramasivam, R. Arumugam, M. Vasudevan and S. Palaniswami, "An Intelligent Self-Tuning PI Type Fuzzy Logic Controller for a Switched Reluctance Motor Drive", Iranian Journal of Electrical and Computer Engineering, Vol.6, No.2, pp.87-97 2007*

[3] *Haga H., Nishiya K., Kondi S., Ohishi K., "High power factor control of electrolytic capacitor less current-fed single-phase to three-phasepower converter," in Proc. Power Electronics Conf., 2010, pp. 443- 448.*

[4] *J. A. M. Blejis,"Continuous conduction mode operationof threephase diode bridge rectifier with constant load voltage," Proc. Inst. Electr. Eng.—Electric Power Appl., vol. 152, no. 2, pp. 359–368, Mar. 2005.*

[5] *HyunjaeYoo, Seung-Ki Sul, "A novel approach to reduce line harmonic current for a three-phase diode rectifier-fed electrolyticcapacitor-less inverter," in Proc. Applied Power Elec. Conf., 2009, 1897-1903.*

[6] *J.Pedra, F. Corcoles, F. J. Suelves, "Effects of balanced and unbalanced voltage sags on VSI-Fed adjustable-speed drives," IEEETransactions on Power Delivery, vol. 20, no. 1, pp. 224-233, Jan. 2005.*

[7] *Chandra Sekar, T., B. Justus Rabi and A. Kannan, 2014. "Harmonics Reduction in Front End Rectifier of Uninterruptible Power Supplies with Active Current Injection" -American Journal Of Applied Sciences, 11(4): 564-569.*

[8] *"Recommended Practice for Monitoring Electric Power Quality," IEEE Std, 1159-2009, Working Group, June 2009.*

[9] *Yufei Zhou, Wenxin Huang, Jianwu Zhao, Ping Zhao, "Tapped inductor quasi-z-source inverter," in Proc. Applied Power Elec. Conf., 2012, 1625-1630.*

[10] *N. Mohan, M. Rastogi, and R. Naik, "Analysis of a new power electronics interface with approximately sinusoidal 3phase utility currents and a regulated DC output," IEEE Trans. Power Del., vol. 8, no. 2, pp. 540– 546, Apr. 1993.*

[11] *P. Pejovic and Z. Janda, "Optimal current programming in threephase high-power-factor rectifier based on two boost converters," NIEEE Transactions Power Electronics., vol. 13, no. 6, pp. 1152–1162, Nov. 1998.*

[12] *F. Oudjama , A. Boumédiène , M. Messirdi and D. Boubekeur 'Comparison of Linear and Nonlinear H-Infinity Controllers for an Electric Vehicle Driven by the Permanent Magnet Synchronous Motor' Vol 12(1): 247-257(2021)*