ANALYSIS OF CMOS and CNTFET SENSE AMPLIFIERS IN SRAM CELL

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Abstract: This paper aims to study different types of current sense amplifiers which are used to read SRAM memory data and to analyze the performance characteristics of CMOS and CNTFET based on parameters like Read delay, Dynamic Power and Static power. The review discusses the working operation of various sense amplifiers. Method to decide feature size of different transistors in sense amplifiers has also been discussed. The paper also focuses on various performance parameters which should be considered during designing of sense amplifiers.

IndexTerms **- CCMSA, CBLSA, HCMSA**

I. INTRODUCTION

SRAMs are used as cache memory hence it must perform at high speed for both read & write operations along with low power consumption. Among all the peripherals of a SRAM memory, sense amplifier plays a major role .It is used to sense or read the data stored or written onto the selected memory bit. The performance of sense amplifiers [1] strongly affects both memory access time and overall power consumption. As the memory capacity is increasing according to the demand for large memory size it give rise to large bit line capacitance which in turn makes memory slower and more energy hungry. A sense amplifier plays the role of sensing the differential voltage generated on the bit line according to the data stored in the memory and accordingly convert the data stored on the bit line/bit line bar to full logic level "1" or "0" which can be read at the output stage. When a memory cell is being accessed for read operation current "IDATA" is produced which removes some of the stored charge (dQ) from the pre-charged bit lines. Since the bit lines are very long, and are shared by other similar memory cells, the parasitic capacitance "CBL" & resistance "RBL" are also large. Hence, the bit line voltage swing (d_{VBL}) caused by the removal of "dQ" from the bit line is very small d_{VBL} = Q/CBL. Sense amplifier is thus used to convert this small voltage swing to a full logic signal. To improve the speed and overall performance of memory it is necessary to understand and analyze different types of sense amplifiers. According to the demand of situation appropriate sense amplifier must be used as every design has its own advantage and disadvantage. Sense amplifiers are classified on the basis of:

1) Circuit Types - Differential and Non Differential.
2) Operation Modes - Voltage, Current and Charge Amplifiers.

A differential sense amplifier distinguishes small signals from noise and starts signal detection faster when compared to non differential sense amplifier. Even though differential sensing requires extra silicon area yet in most of the design the use of differential amplifier allows combining very high packaging density with reasonable access time and low power consumption. The rest of the paper is organized as follows. Section II describes the different current sense amplifiers, Section III describes the simulation results and Section IV describes the conclusion of this paper.

II. TYPES OF SENSE AMPLIFIERS

There are different types of sense amplifiers that can be used in SRAM, but in this paper the following three sense amplifiers are designed:

1. Conventional Current Mode Sense Amplifier (CCMSA)
2. Clamped Bit Line Sense Amplifier (CBLSA)

3. Hybrid Current Mode Sense Amplifier (HCMSA)

The simplest Voltage Sense Amplifier is the differential couple. When a cell is being read, a small voltage swing appears on the bit line which is further amplified by differential couple and use to drive digital logic. However the bit line voltage swing is becoming smaller and is reaching the same magnitude as bit line noise, the voltage sense amplifier become unusable.

The fundamental reason for applying current mode sense amplifier in sense circuit is their small input impedances. Benefits of small input and output impedances are reductions in sense circuit delays, voltage swings, cross talking, substrate currents and substrate voltage modulations. A differential charge transfer amplifier takes advantage of the increased bit-line capacitance and also offers a low-power operation without sacrificing the speed.

Conventional Current Mode Sense Amplifier

In advanced memories the capacitances of the bit line is increasing due to technology scaling and the increasing number of cells attached to the column. In such memories voltage mode cannot keep up to their performance thereby leading to the need for faster sensing techniques that are not affected by the bit line capacitance. Current sensing is typically 17-20% faster than voltage sensing. Current Sense Amplifier can be enabled faster than voltage mode, as current sensing does not depend on differential discharging of large bit-line capacitance. The bit-line swing for current sensing is 35-40% less than the voltage mode, but the energy saved with reduced bit-line swing is compensated by the static power dissipation of the current sense amplifier. Current mode sense amplifiers are applied to reduce the sense circuit delays as they provide low common input/output impedances. The small input impendence presented to the bit-lines result in reduced voltage swings, cross-talk and substrate currents.

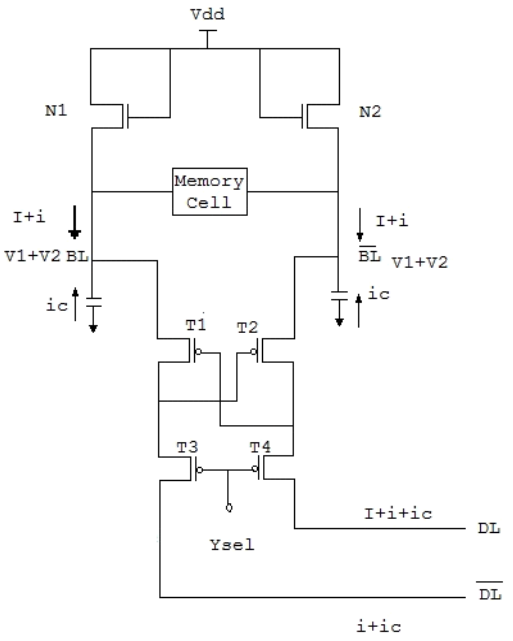

Fig. 1: Conventional Current Sense Amplifier using CMOS

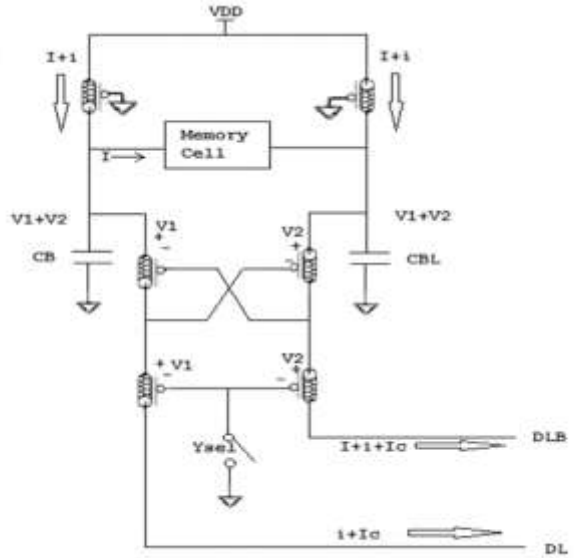

Fig.2: Conventional Current mode Sense Amplifier using CNTFET

Current mode sense amplifier is used to detect the current difference between the bit lines to determine whether a '1' or '0' is stored in the memory cell. It directly measures the cell read current and transfers to the output circuits. This approach can overcome the restriction of gain reduction brought on by voltage mode sense amplifier at low power supply voltage. The simplest structure of the current mode sense amplifier for CNTFET and CMOS are Shown in Fig.1and Fig. 2. The Conventional Current Sense Amplifier basically consists of four equal sized PMOS transistors as shown in Fig.1 & 2. It features a current sensing character since it represents a virtual short circuit to the bit lines, which transfer the cell

current directly to the output circuits. If memory cell stores '0' then when it is accessed, it draws some current. The difference in the current flowing through both branches will be equal to cell current. The current in DLB is higher than current in DL as shown in Fig. 1 & 2. This differential current is used to find whether the stored bit in the SRAM cell is either 0 or 1.

Hybrid Current Mode Sense Amplifier (HSA)

In the design of new current-sensing data paths, two different current-sensing circuits are employed at bit lines and data lines, respectively. Hence a new hybrid current-mode sense amplifier is formed. The simplified new current-mode sense amplifier data path is shown in Fig.3 and Fig.4.

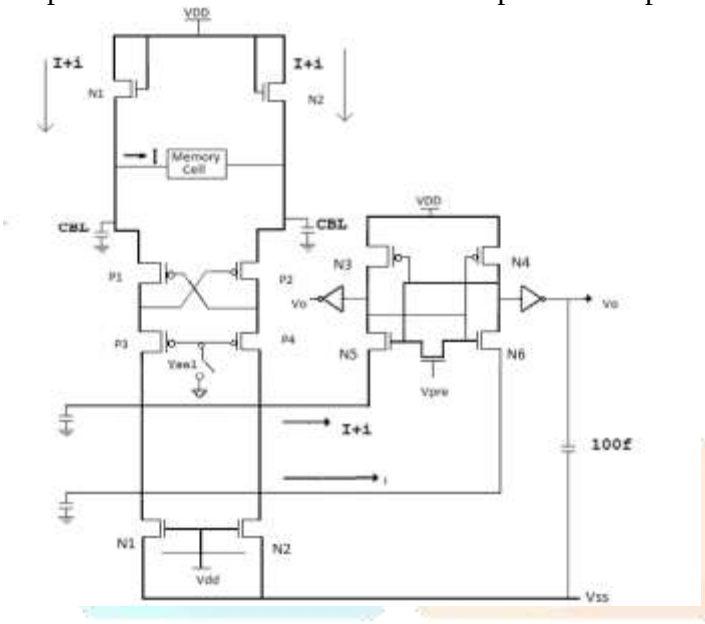

Fig. 3 Hybrid Current Mode Sense Amplifier using CMOS

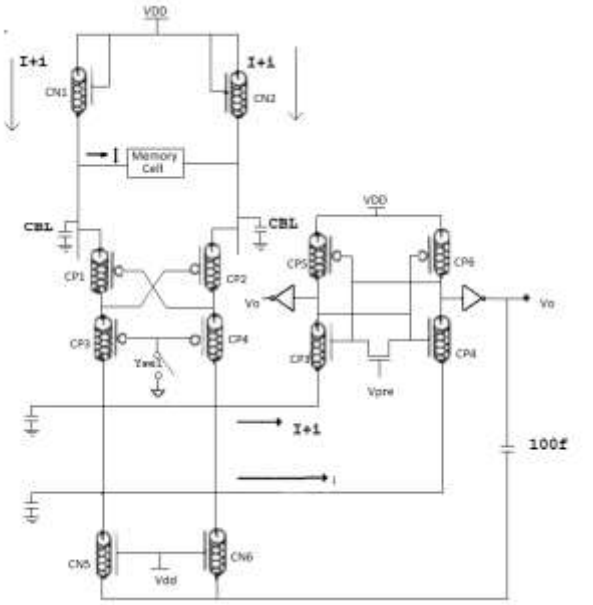

Fig. 4 Hybrid Current Mode Sense Amplifier using CNTFET

The parasitic capacitance associated with the long bit line is characterized by a large capacitance *CBL*. The current conveyor used in the conventional current-mode sense-amplifier is adopted for column sensing. The pre-equalizing device is omitted, because the current conveyor intrinsically keeps the bit lines at equal potentials once *YSEL* is initiated. The current conveyor consists of four equal-sized PMOS transistors that fit in the column pitch well. The bottom two transistors can even double up as a column-select device, thus reducing the propagation delay. The current conveyor is just a current transport circuit with no gain. To speed up the read operation, a cross coupled circuit which has a regenerative effect is proposed for the common data-line pair. The new cross coupled circuit is not only required to present a virtual short-circuit at the inputs but must also be able to convert the cell signal current to a CMOS voltage signal directly. The conventional CMOS cross coupled latch is modified to respond to current signals similar to the technique used in the clamped bit-line current-mode sense amplifier. The inputs to the current-mode cross coupled latch are at the sources of n-channel transistors N3, N4. Owing to the low impedance at the input nodes, the current signals at the data lines are injected to the cross coupled latch without charging and discharging of the data-line capacitors. Therefore the sensing speed is insensitive to both bit-line and data-line capacitances. During the read operation, device N5 of the current-sensing CMOS cross coupled latch is first turned on to pre-charge the output nodes to equal potentials. A particular memory cell is accessed when the RS line is activated. A complementary node of the cell at low level draws current from the bit-line load. Differential current signals then appear at the common bit lines bit and bit. The current conveyor transports the differential currents to the data lines. Sufficient time is provided to allow differential currents to appear at the data lines before the pre-equalising device, N5, is turned off. Once N5 is turned off, the differential currents flow through N3 and N4, charging the small equivalent capacitances at the drains of N3 and N4 respectively. A small differential voltage *AV* will appear across the intermediate nodes V3 and V4 of the current sense amplifier. The positive feedback effect of the cross coupled circuit amplifies the small

differential voltage to CMOS-signal level. Owing to the output node, capacitance is much lower, and the response speed of the cross coupled latch is very high.

Clamped Bit Line Current Mode Sense Amplifier (CBLSA)

The circuit is able to respond very rapidly, as the output nodes of the sense amplifier are no longer loaded with bit line capacitance. The input nodes of the sense amplifier are low impedance current sensitive nodes. Because of this the voltage swing of the highly capacitance bit lines change is very small. The improvement in the driving ability of output nodes due to positive feedback and the small difference can be detected and translated to full logic. It is almost insensitive to technology and temperature variations. The main limitation of this circuit is that the bit lines are pulled down considerably from their pre-charge state through the low impedance NMOS termination. This results in significant amount of energy consumption in charging and discharging the highly capacitive bit lines. Also, the presence of two NMOS transistors in series with the cross-coupled amplifier results in an increase in the speed of amplification.

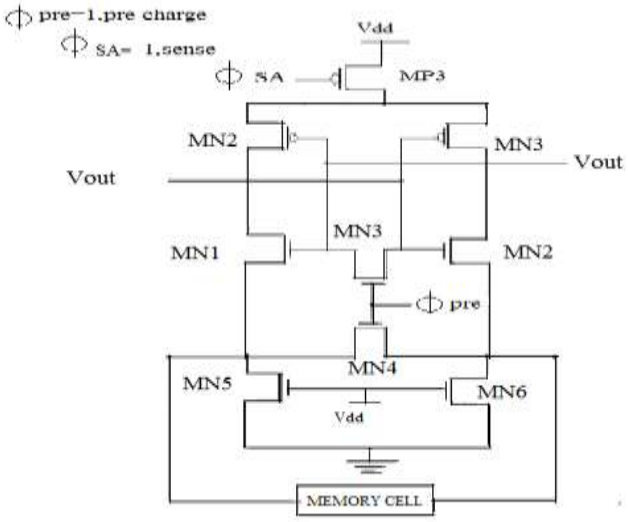

Fig.5 Clamped Bit Line Current Mode Sense Amplifier using CMOS

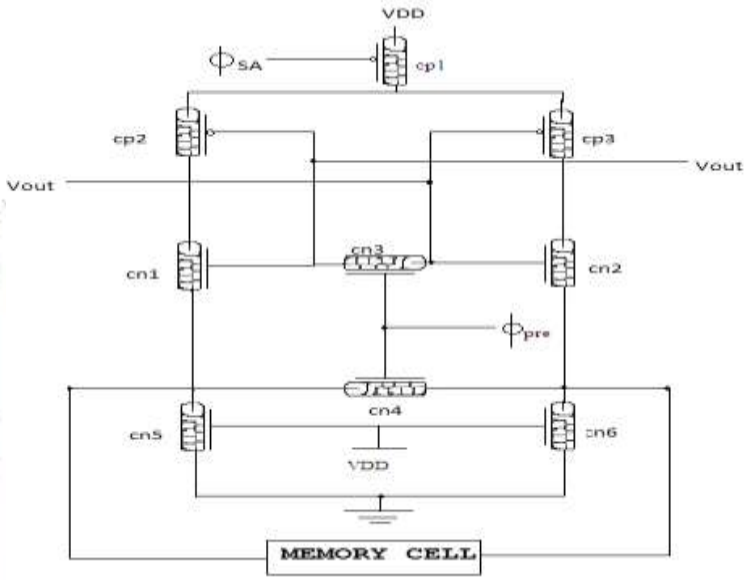

Fig.6 Clamped Bit Line Current Mode Sense Amplifier using CNTFET

The circuits shown above are Clamped Bit Line Current Mode Sense Amplifiers for CMOS and CNTFET. The sense amplifier operates in two phases: pre-charge and sense signal amplification. To begin a memory access, the large-geometry device M9 is turned on, providing power to the sense amplifier. Devices M7 and M8 are on during pre-charge, forcing the bit lines to equal potentials. The operating current of the sense amplifier is determined by the sizes of M 1- M4, and is designed to charge the bit lines to a potential of approximately 0.1 V. Device M8 is also on during pre-charge, forcing the sense amplifier output nodes to equal voltages. The output voltage is approximately 2 V in this design and is dependent upon the W/L ratios of M 1- M4. For the case where I >Iacurrent A I = ID- IRE, will flow through the pre-charge device M7 in the CBLSA. For a conventional sense amplifier (CSA), AZ would flow through a pre-charge device equivalent to M8. At the end of the pre-charge cycle, M7 and M8 are turned off, and Ml-M4 then acts as a high-gain positive feedback amplifier. Due to the positive feedback, the impedance looking into the source terminal of either M1 or M2 is a negative resistance, which causes M1 and M2 to begin sourcing a portion of the difference current AI when M7 is turned off. The difference current flowing through M1 and M2 flows through the small equivalent capacitance at the drains of M1 and M2, giving rise to a AV across the output nodes of the sense amplifier. The initial trajectory for the magnitude of the voltage difference between the drains of M1 and M2 is given approximately by I_dAV/dtl= 2AZ/Cd where C, is the total capacitance at the drain node of M1 or M2. This trajectory is followed for a short time, and then the resulting differential voltage at the output of the sense amplifier is rapidly amplified by the positive feedback of the latch, driving Vow+ high and VOuT- low, for the case of positive Al. The speed of this

clamped bit-line sensing scheme will be high due to two primary factors. First, since the input of the sense amplifier is a low-impedance current sensitive node, the highly capacitive bit lines change by only a few tenths of a volt during the sensing operation. Secondly, the output nodes of the sense amplifier are no longer loaded with the bit-line capacitance and the sense amplifier is able to respond very rapidly. In addition, not charging and discharging the bit-line capacitances during cell access reduces power consumption and internal power supply "bounce," increasing the reliability of circuit operation. Note that the bit lines will be completely discharged at the end of the sensing operation, since the current in the sense amplifier goes to zero in the latched state.

III SIMULATION & RESULTS

The various sense amplifier circuits are implemented in HSPICE (H Simulation Program for Integrated Circuit Emphasis) and their performance is evaluated by calculating various parameters like read delay, static power and dynamic power of the circuit in the 32nm technology with the power supply V_{DD}=1V.
The circuit is designed in such a way that it has very less read delay which implies that it takes very less time to read the data.

Conventional Current Mode Sense Amplifier: CMOS CMSA

The Current Sense Amplifier designed using CMOS technology (as shown Fig.1) and same is simulated using HSPICE. The Fig.7 shows the output waveforms for the current sense amplifier. v(q),v (bl),v(op) shows the waveforms at Memory Cell, Bit line and sense amplifier output respectively.

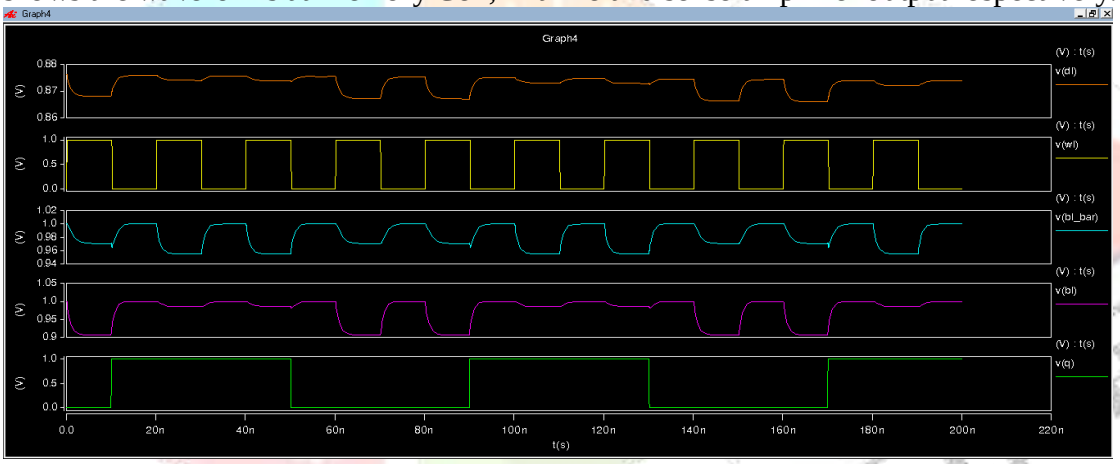

Fig. 7. Simulated waveforms of CMOS Current Sense Amplifier

CNTFET CSA: The Current Sense Amplifier designed using CNTFET technology (as shown Fig.2) and same is simulated using HSPICE. The Fig.8 shows the output waveforms for the current sense amplifier. v(q), v(bl), v(op) shows the waveforms at Memory Cell, Bit line and sense amplifier output respectively.

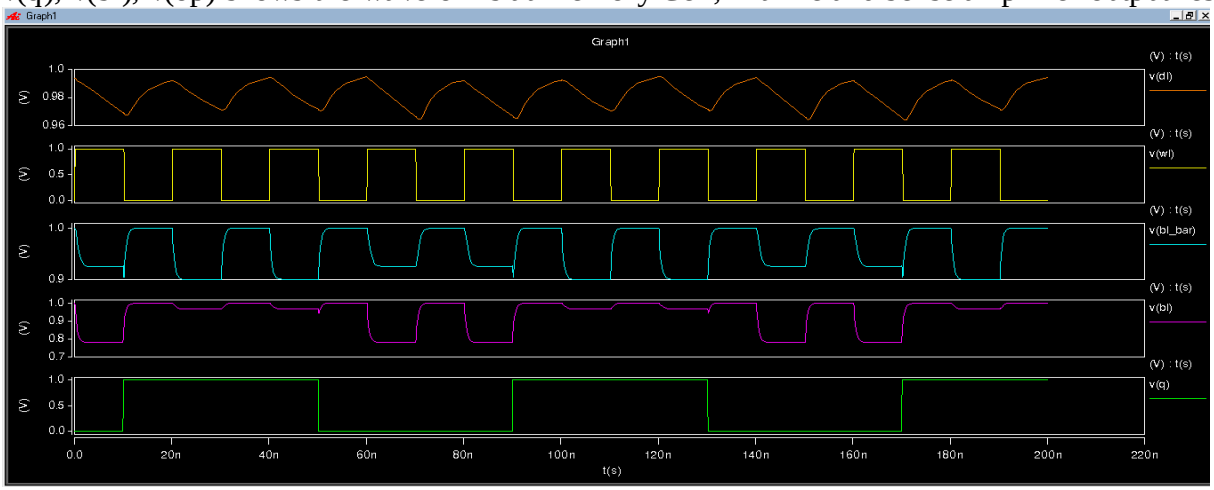

Fig.8 Simulated waveforms of CNTFET Current Sense Amplifier

Hybrid Current Mode Sense Amplifier: CMOS HSA

The Hybrid Current Sense Amplifier designed using CMOS technology (as shown Fig.3) and same is simulated using HSPICE. The Fig.9 shows the output waveforms for the current sense amplifier. v(q),v(bl),v(dlb) shows the waveforms at Memory Cell, Bit line and sense amplifier output respectively.

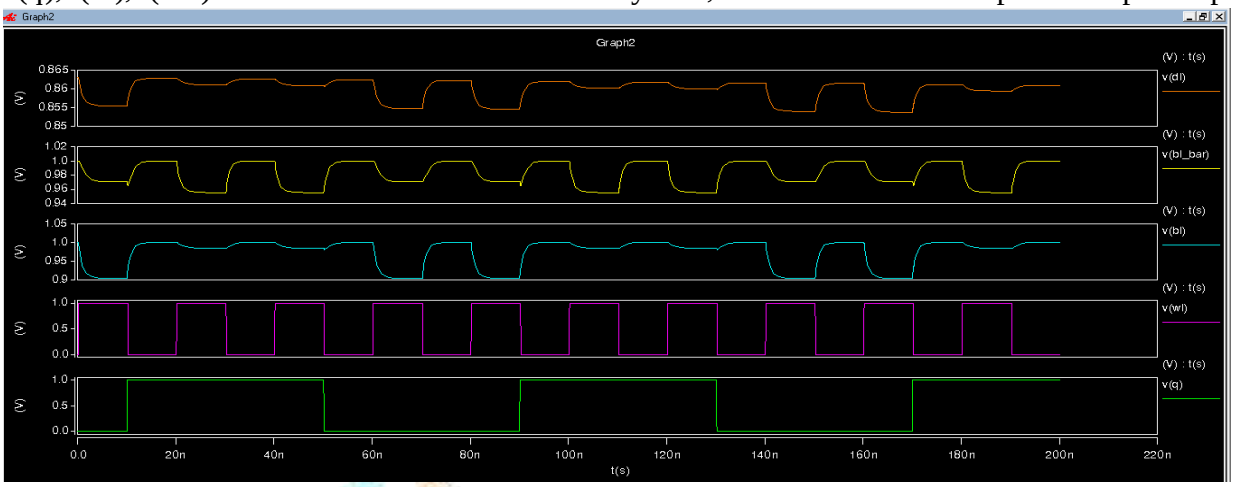

Fig. 9: Simulated Waveforms of CMOS Hybrid Current Mode Sense Amplifier

CNTFET HAS : The Hybrid Current Sense Amplifier designed using CNTFET technology (as shown Fig.. 4) and same is simulated using HSPICE. e Fig.10 shows the Static and dynamic power dissipation and read delay for the CNTFET based Hybrid Current Sense Amplifier.

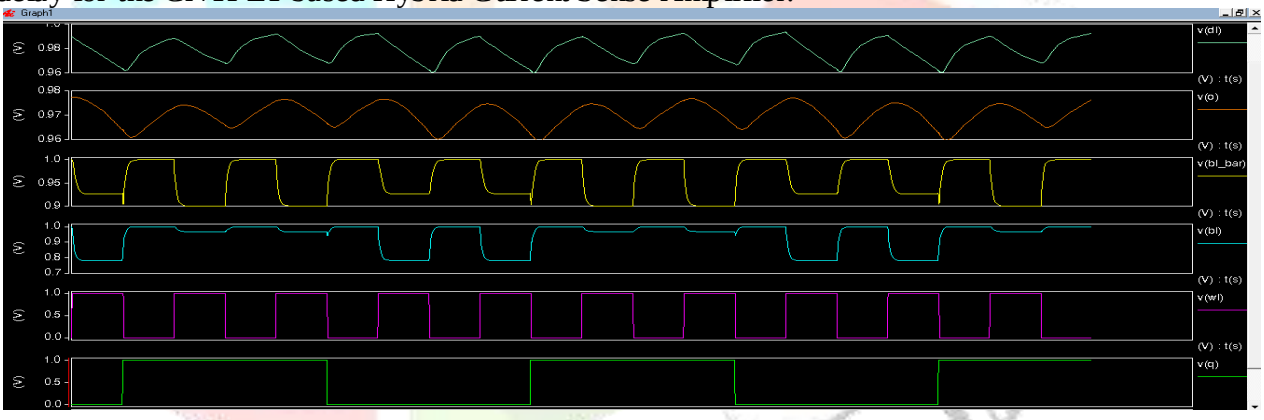

Fig.10: Simulated Waveforms of CNTFET Hybrid Current Mode Sense Amplifier

Clamped bit line Current Mode Sense Amplifier: CMOS CBLSA

The Clamped Bit Line Current Sense Amplifier designed using CMOS technology (shown Fig. 5) and same is simulated using HSPICE. The Fig.11 Shows the output waveforms for the Clamped Bit Line current sense amplifier and v(q),v(bl),v(n) shows the waveforms at Memory Cell, Bit line and sense amplifier output respectively.

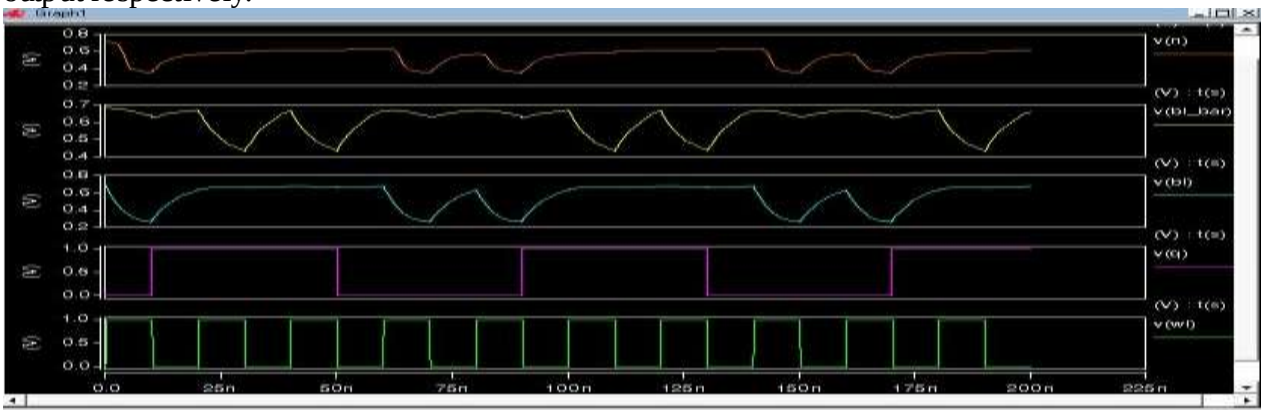

Fig.11: Simulated Waveforms of CMOS Clamped Bit Line Current Mode Sense Amplifier

CNTFET CBLSA : The Clamped Bit Line Current Sense Amplifier designed using CNTFET technology (as shown Fig. 6) and same is simulated using HSPICE. The Fig.12 Shows the output waveforms for the Clamped Bit Line current sense amplifier. v(q),v(bl),v(n) shows the waveforms at Memory Cell, Bit line and sense amplifier output respectively.

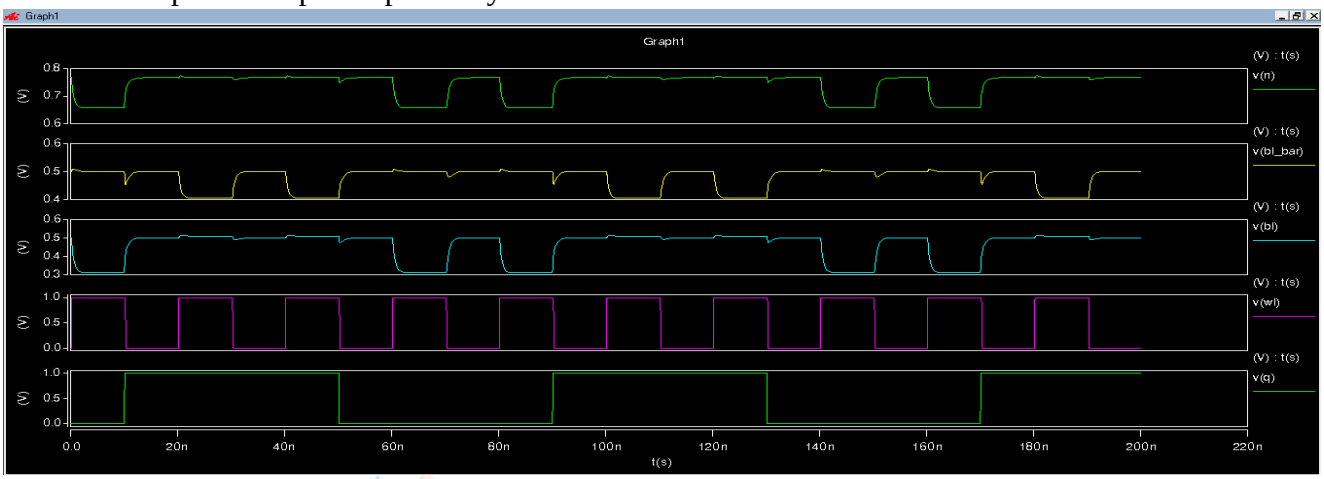

Fig. 12: Simulated Waveforms of CNTFET Clamped Bit Line Current Mode Sense Amplifier

Table: 1 Comparison of Different Parameters among CNTFET and CMOS

Parameter	Conventional current mode sense amplifier		Hybrid current mode sense amplifier		Clamped bit line current mode sense amplifier	
	CMOS	CNTFET	CMOS	CNTFET	CMOS	CNTFET
Read delay (ns)	47.4	2.37	18.4	0.132	490	13.9
Dynamic power(uw)	27	9.343	27	9.04	6.49	0.622
Static power (pw)	2.35	0.19	2.38	0.18	0.583	0.013

The Table:1 shows the tabulated comparison of different parameters among the CMOS and CNTFET SRAM different current mode sense amplifiers.

- In Conventional Current Mode Read delay, Static Power and Dynamic Power is 85%, 87.6%, 97.1% better in CNTFET when Compared to CMOS respectively.
- In Hybrid Current Mode Read delay, Static Power and Dynamic Power is 86.06%, 86.77%, 97.01% better in CNTFET when Compared to CMOS respectively.
- In Clamped Bit line Current Mode delay, Static Power and Dynamic Power is 64.74%, 56%, 90.19% better in CNTFET when Compared to CMOS respectively.

This Comparison shows that Hybrid Current Mode Sense Amplifier (HSA) is better than Conventional current mode and Clamped Bit Line current mode Sense Amplifiers in Read delay with a percentage of 94.43% and 99.05% respectively.

In the view of dynamic power Clamped Bit Line current mode Sense Amplifier is better than Hybrid current mode Sense Amplifier with a percentage of 50% and Conventional Current mode Sense Amplifier with a percentage of 50.62% respectively.

If the critical parameter is Read delay Hybrid Current mode Sense Amplifier (HSA) is preferred to all other Current mode Sense Amplifiers.

If the critical parameter is Dynamic power Clamped Bit Line current mode Sesne Amplifier (CBLSA) is preferable than Conventional and Hybrid Current mode Sense Amplifiers.

IV Conclusion

Design Analysis of different Sense Amplifiers and its circuit description is discussed and the results of Designed circuits are simulated and their corresponding output waveforms are obtained successfully.
This paper presents the performance evaluation of sense amplifier topology– Sense Amplifiers. The obtained Results shows better performance in terms of static, dynamic power and power dissipation in CNTFET design compared to CMOS design. Among all the sense amplifiers Hybrid Current mode Sense amplifier circuit is the best circuit, since it has less read delay and less static, dynamic power consumption.
It would be concluded that CNTFET comes up with extremely high efficiency compared to MOSFET because of its less power dissipation and less static, dynamic power.

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