Analysis and review of all Relay Processes and Design Optimization for Low Voltage High Speed Operation

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Abstract: This paper focuses on relay process and design optimization. With optional additional lithography steps, we can achieve a more robust process required for eventual device scaling, highly reduced device footprint area, and the ability to form interconnects to fabricate circuits. Improved relay designs minimize parasitic electrostatic force issues and enhance functionality. The process flow is optimized to achieve the lowest switching voltages, while still ensuring reliable turn-off and avoiding stiction. New device concepts increase device functionality to reduce the number of structures required to achieve a certain function, and provide a new paradigm for designing circuits using relays.

Index Terms - electrostatic force, digital integrated circuits, lithography, interconnects, parasitic effects, stiction.

I. INTRODUCTION

The ideal switching characteristic of zero off-state leakage and abrupt switching behavior of relays makes it attractive for DIC (digital integrated circuit) applications as chip power density has become a major challenge in recent years. A robust and reliable 4Terminal (4T) relay technology, having high yield (>95%) and excellent endurance (>1010 on/off cycles) has been demonstrated previously (1). Indeed, ideal switching characteristic is demonstrated with SS < 0.1mV/dec and immeasurably low IOFF (<10-14A). However, the process technology and design are not optimized. The device footprint is unnecessarily large, and the release process relies on a timed etch. Parasitic electrostatic effects were found and operating voltages remain too large, making it difficult to implement complex logic circuits with the technology. In order to fully realize the promise of relays as an alternative to CMOS for low power digital circuits, the relays need to be able to operate with voltages <1 V, i.e. with minimal hysteresis. The hysteresis voltage sets the minimum VPI where the relays can still turn off (i.e. when VRL=0V, VPI = hysteresis voltage).

II. 5 MASK/7 MASK PROCESS

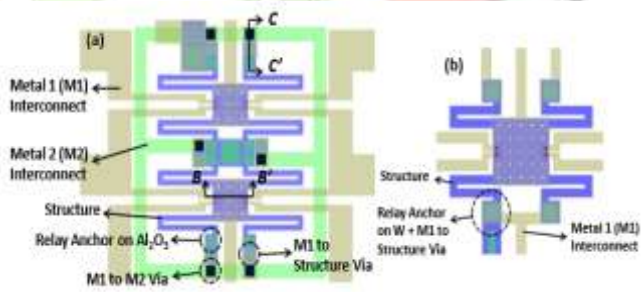

Fig 1: Layout view (1) illustrating improved anchor and interconnect design on dual source/drain devices. (a) An inverter circuit. (b) Device anchored directly on W (M1 interconnect).

As an attempt to design for lower voltages, an improvement to the process is required. The 4-mask process studied in (1), is simple and sufficient to fabricate the first prototype devices. However, it can be improved to facilitate miniaturization and to fabricate large circuits reliably. In the original process, the structural layer is anchored on the sacrificial material. As a result, the release time needs to be kept short and the printed anchor size needs to be large to make sure the anchors survive. With scaling, gap thicknesses are expected to be smaller and a long release time may be required. A timed release requirement could potentially limit scaling. Large anchor regions also consume a lot of area, unnecessarily increasing the device footprint. In fact, the anchors (50 µm × 50 µm each) make up >50% of the total device area (120 µm × 150 µm) in the 1st generation design. The location and size of the actual anchor is not lithographically fixed. It is determined by the lateral etch distance of the sacrificial oxide underneath, potentially an added source of process-induced variation in the effective spring constant. An extra mask (i.e. a 5-mask process) is needed to form a more reliable anchor and to electrically connect the structural layer and the fixed electrodes to build circuits. The new anchor and interconnect design are illustrated in Figure 1. Anchors can be formed directly on the Al2O3 substrate dielectric or the W electrodes (M1 layer) to form an electrical connection for circuit routing. The anchor size is lithographically defined, the HF vapor etch time is not limited, and large anchors are not required. An anchor size of 10 µm × 10

µm is adequate, reducing the device footprint to 68 µm × 78 µm. An optional two additional masks (i.e. a 7-mask process) could be used to provide an additional layer of interconnect (M2 layer) for larger circuits.

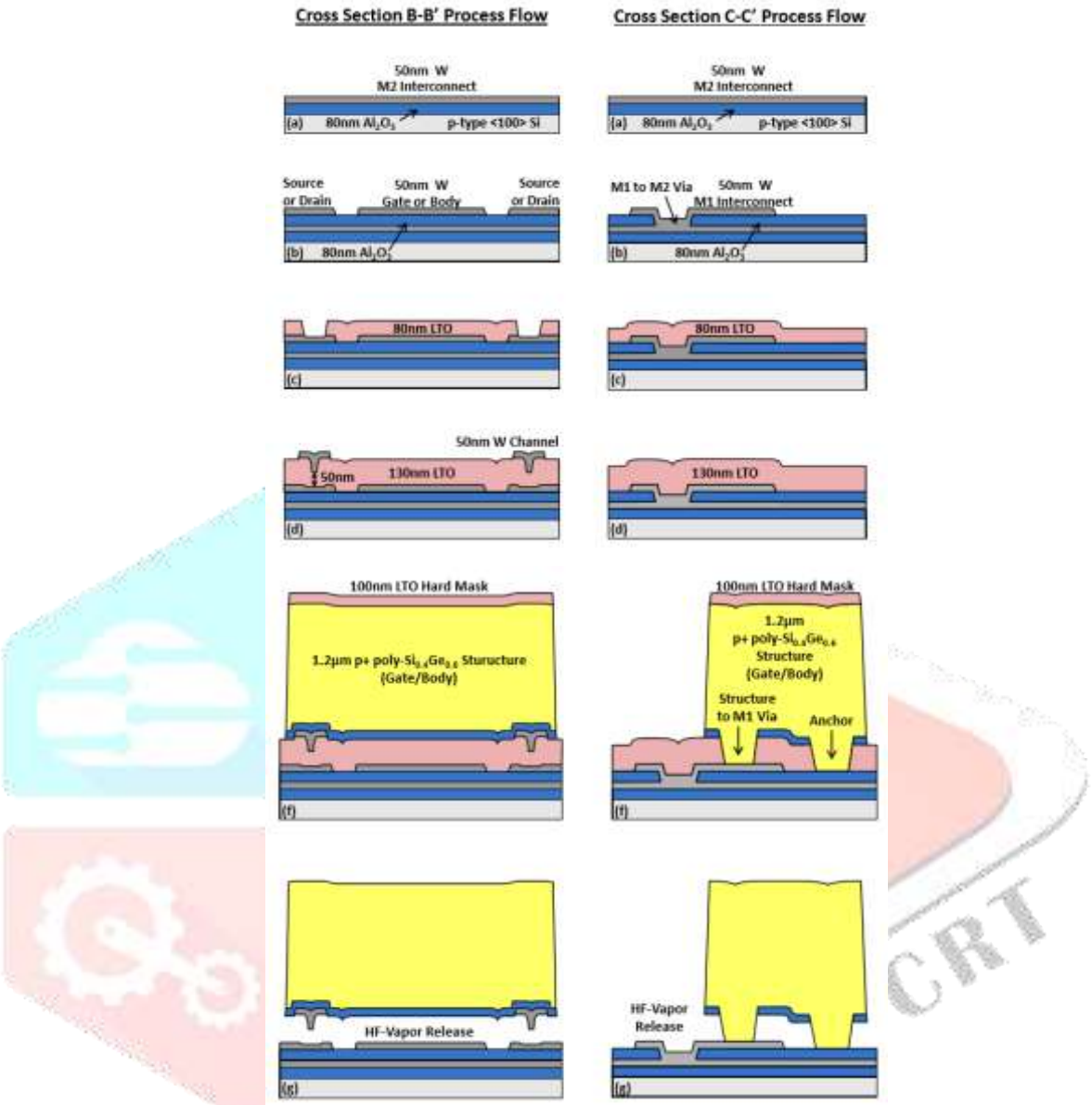

Fig 2: Illustrations along cross section B-B' and C-C' in Figure 1, showing a 5 mask/7-mask process flow for fabricating a four-terminal relay.

The improved process is illustrated in Figure 2 (1). On a starting silicon wafer substrate, a layer of Al2O3 (80 nm) is deposited by ALD to form an insulating substrate surface. A 50 nm tungsten layer is deposited by sputtering and patterned to form Metal 2 (M2) interconnect layer. Another 80 nm layer of Al2O3 is deposited by ALD as the interlayer dielectric (ILD) and M1-to-M2 via holes are opened. A second tungsten layer is deposited by sputtering and patterned to form Metal 1 (M1) interconnect, the gate/body, source, and drain electrodes. Next, a first sacrificial layer of SiO2 is deposited via LPCVD and patterned to define the contacting regions. Due to overetching, the surface of the tungsten source/drain electrodes is slightly recessed. A second sacrificial layer of SiO2 is deposited. The 2nd sacrificial layer thickness defines the contact dimple gap, whereas the total thickness of the two sacrificial layers defines the actuation gap. Next, a tungsten layer is deposited and patterned to form the channel. Afterwards, a layer of Al2O3 is deposited to form the insulating gate/body oxide layer, followed by definition of structure-to-M1 via holes. P+ poly-Si0.4Ge0.6 structural layer is deposited by LPCVD and patterned along with the gate/body oxide layer with the aid of SiO2 hard-mask layer. The structures are released by selectively etching away all of the SiO2 in HF vapor. As an optional step, an ultra-thin layer of TiO2 can be conformally deposited by ALD for reliability improvement.

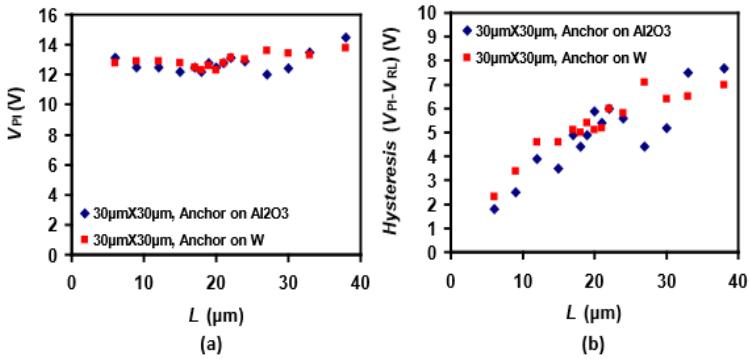

Fig 3: Comparison of a 4T relay design anchored on Al2O3 and W showing (a) VPI and (b) hysteresis voltage.

It should be noted that for all the designs the gate and body electrodes are interchangeable. It is beneficial for circuit design to be able to use either the movable (SiGe) electrode or fixed (W) electrode to actuate the relay. Measurements are performed to see if anchoring on Al2O3 or W would make a difference for a range of different flexure lengths (L) (Figure 4.3). Very similar VPI and hysteresis are measured. Thus, the relay anchor can also be used simultaneously as a structure-to-M1 connection to save area.

III. CONCLUSION

In this review paper, various relay processes have been discussed. From the work, it is quite clear that 5-Mask and 7-Mask processes are more stable and hence can be implemented for low voltage designs of Ultra fast low energy digital integrated circuits. Also a detailed construction process has been studied in this paper.

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