Improved Design Of Low Power Precision Scalable Approximation Multiplier

M. Zahir Ahmed, Lecturer in Physics, Osmania College (Autonomous),Kurnool-518001

Andhra Pradesh, India.

ABSTRACT:

Approximation equations are techniques that can be used to reduce power consumption and increase accuracy. Multiplication is an important function of many error applications. The proposed precision controllable multiplier can be dynamically adjusted to meet the requirements. It can produce long-life anti-aging products. The proposed algorithm can adjust the length expansion to achieve good accuracy. The concept of wood compactor consists of partial wood product estimated by the carry mask collector. Partial wood products are calculated from the demand balance. The approximate number includes ATC and carries an additional mask. Both ATC and CMA have low power consumption and simple circuit design.

Index terms: ATC, CMA, Lower power consumption. CKT design

1.Introduction:

In general, the processing of photos and applications can avoid minor errors. This function is often used in high complexity applications where calculation accuracy is not an issue. However, it can also be used to reduce energy consumption. Predictive code is a technique that can reduce power consumption and increase trust against unauthorized use. This technique is often used for crime. Different types of crimes have different requirements. If the correct partition is set, power will be discarded if not needed. If it can be dynamically reconfigured, the estimated multiplier should be the same as that required for different level programs [2]. This article is designed to create a multi probabilistic design that can check the correctness of a function. This design can be configured to work seamlessly with a variety of transport propagation collectors. proposed a carry-masked adder that allows programmers to modify the propagation function [3].

Many increasingly popular applications, such as image processing and authentication, are tolerant to minor errors. These applications are computationally demanding and division is their main arithmetic operation, creating the opportunity to trade off correct numbers for lower power consumption. Estimation is a good method for error applications because it can sacrifice accuracy for efficiency and currently plays a major role in these applications [4]. Different penalty applications have different requirements, such as applying different procedures to the application. If the right balance is achieved, power is wasted when the correct requirement is not high. This means that the estimation equations must be adjusted to accommodate the differences in accuracy between different methods and applications. This article focuses on an approximate model equation whose accuracy can be dynamically controlled. A carry-masked adder (CMA) is intended to be dynamically configured to operate as a regular carry-propagated adder (CPA), a series of bit-parallel OR gates, or a

combination of both. This configurability is achieved by masking the carry propagation: the CPA of the last stage of the multiplier is replaced by the CMA strategy [5]. Approximately one wood compactor is used to reduce the mixed layer depth of a portion of the wood product. Our approach introduces a concept that represents the power and need to be realistic, facilitating Partial Product Reduction (PPR) when necessary.

2. Existing system:

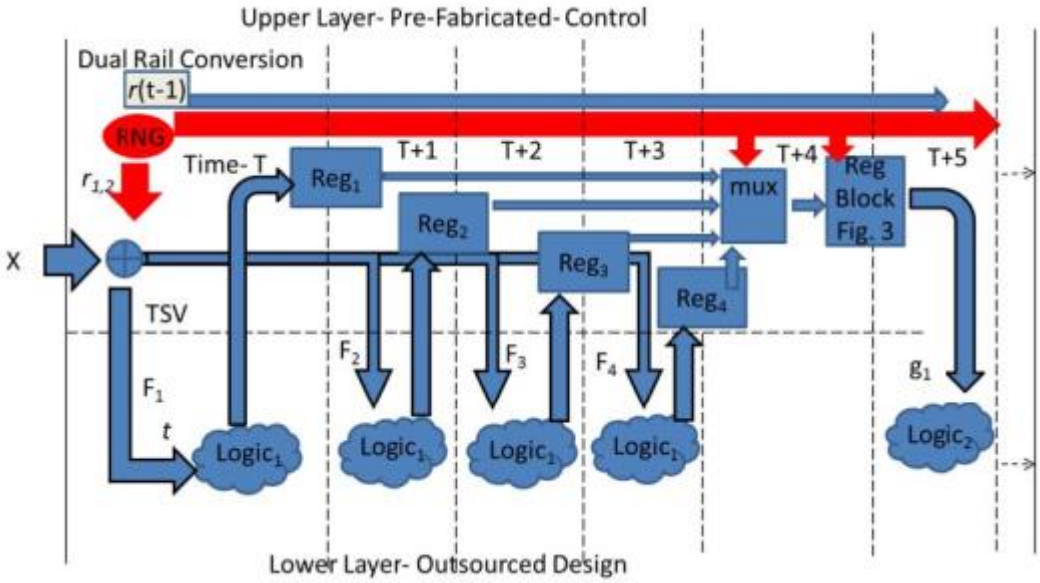
Ultra-fast collectors hybrid PPFCSL and hybrid Han-Carlson are also discussed in the literature. As reported, the ultrafast collector is the fastest collector, although our gate is slower than Han-Carlson. However, it uses twice the gate area of the Han-Carlson adder. On the other hand, the hybrid Han-Carlson collector is designed with two Brent-Kung stages at the beginning and end and a Kogge-Stone stage in between. This is slightly slower than the Han Carlson adder (two gates slower), providing a 10% to 18% reduction in gate complexity [6].

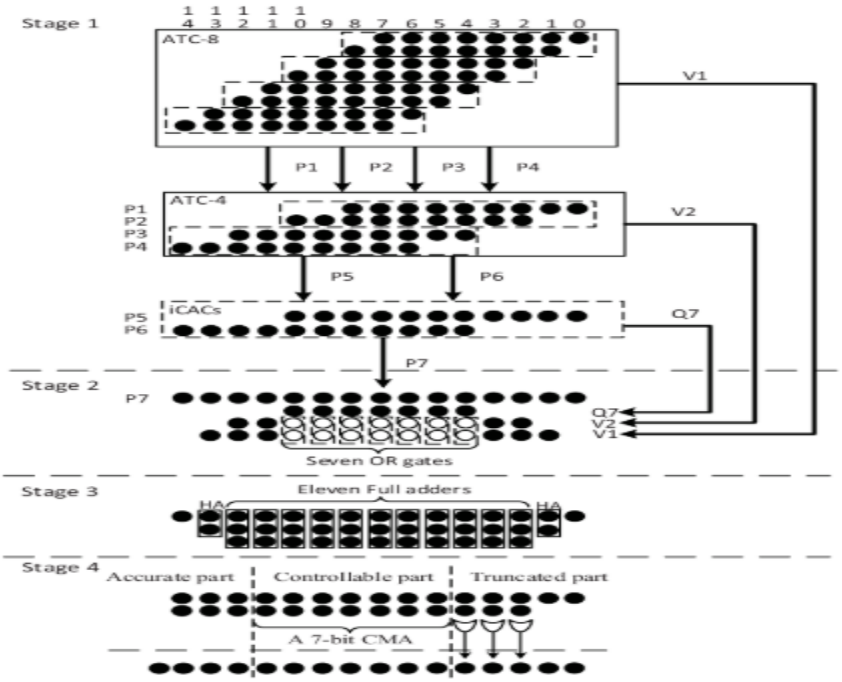
The current method excites the content with different results by changing some of the product. These results are identified and then estimated using the theoretical framework. As a sensitivity control, the partial output is written to produce a signal using an OR gate. The signals they produce have a significant impact on the error rate. The maximum number of "correct" characters that can be grouped to produce correct results is limited to "4".

3. Proposed system:

To reduce area and latency, existing techniques use OR gates instead of XOR summation on half adders. This leads to errors in calculations. In the case of all adders, an OR gate replaces the XOR gate in the addition calculation. In a 4-2 compressor, one XOR for every three XOR gates is replaced by one OR gate. This resulted in an error in 5 out of every 16 cases [7]. Using these modules, two multipliers were created. In the first equation; The second multiplier reduces area and circuitry by using approximately at least n-1 OR gates. Both equations are very easy to create but do not give accurate results for higher values. • Current systems are designed to increase latency. The proposed distribution can be seen in the image. In this model [8], we can use 16 bit adder by using 8-2 AC in half generation and final addition stage after completion of OR gate operation process. The implementation of above equation is created in Verilog code and then we can test it using Xilinx 14.7. ¤¤The proposed method is used to reduce the delay level.

3.1.SYSTEM ARCHITCTURE:





In the half adder concept, when mask_x is 0, S is equal to x OR y and Cout is equal to 0. It cannot be used as a half adder when mask_x is on. It is enabled by default [9]. The practical adder is similar to the half adder in that it can be used as an absolute adder when mask_x is enabled. Outputs Cout or S depending on the options.

4.Product design:

PPR using tree adder and Additional use of CPA to generate the final results. Power consumption and competition in the circuit are determined by PPR and the main path of competition is determined by extending the carry chain in CPA [10]. Two types of approximate compressors are designed for approximate multipliers. These compressors exhibit short latency and low power consumption compared to precision compressors whose implementation can produce high quality graphics with low power consumption [11]. It is

similar to k-bit CPA with half adders with carry mask and full adders with carry mask. In the half adder concept, when mask_x is 0, S equals x OR y and Cout equals 0. It cannot be used as a half adder when mask_x is on. It can also be enabled by default. The practical adder is similar to the half adder in that it can be used as an absolute adder when mask_x is enabled. Outputs Cout or S depending on the options. The equivalent circuit of the half adder and the dashed box represents the equivalent circuit of a 2-input XOR gate. Since there is a 2-input NAND gate in the dotted box, we reuse it and add an INV gate to generate the Cout carry signal. The outputs of the 2-input NAND and OR gates in the dashed box are called u and w respectively. Table 1 is the real table of the equations of the half adder. This means that if you check and control to 1, the carry propagation will be covered and the sum s will be equal to OR b. The sum s = a OR b is different from the real sum (= a XOR b) except that both a and b are 1. The selection of the correct and approximate values can be done by controlling the signal used to control you to make NAND b or make it 1 and give a short delay. The proposed carry mask adder can be dynamically controlled by the set of controllability parameters [12]. Each iCAC row has an incomplete PP: for example, the PP at position 0 in the first row of the first iCAC block in ATC-8 is incomplete, and the PP at position 8 in the second row. In the first stage, the eight lines of the PP are reduced to four lines (P1, P2, P3 and P4) and a load vector (V1) by the ATC-8. ATC-4 also reduces the four lines to two lines (P5 and P6) and another load vector (V2). Then the last line of iCAC processes P5 and P6 and generates P7 and Q7. In summary, the first stage compresses 8 x 8 PP into four columns (P7, V1, V2 and Q7) using ATC-8, ATC-4 and seven iCAC rows. In Level 2, all positions from 4 to 10 have 4 PP. To obtain the slowest method, an OR gate is used to estimate the sum of V1 and V2. The empty circles in V1 and V2 represent the bits calculated using the OR gate. There must be seven OR gates in total, and four rows are compressed into three rows. In stage 3, the three rows are compressed into two rows using full adders and half adders. Items 1 and 13 require two half adders, and items 2 through 12 require eleven adders. Additional CPA is required after PPR to obtain the final result. For an 8-bit Wallace tree multiplier, the length of the CPA is 13. Since the low-order bits are not important for precision, bits 0 through 4 are defined as truncation and our OR gate is used to produce the results. Items 2, 3, and 4 of the final result. Since there is no lift in the truncation part, the CPA length is reduced to 10. Since the above items are the most important for accuracy, items 12 through 14 are identified as correct and three additional facts are used to form the value of these items for the final result.

5.CONCLUSION:

This paper presents an approximator with control accuracy that uses less energy and has shorter delay than traditional models. Its dynamic controllability is achieved by applying CMA. This multiplier is measured at the circuit and application level. In signal processing and image processing, approximation is often used to solve complex and uncomplicated tasks. This paper presents a true scalable approximator multiplier to reduce power consumption and shorten the critical path. The proposed carry mask adder can be dynamically controlled through controllability techniques. Carry mask adders are commonly used for home computers. The

proposed CMA performs quality control through the use of masking devices. Simulation results of the carry maskable adder are shown. The use of these adders is suitable for the computation of precision multipliers. Experimental results show that the demand multiplier can save energy and increase speed while maintaining a smaller area than Wallace tree multipliers. Moreover, for the same accuracy, the proposed number matching achieves greater improvement in power consumption and significant latency over other previous matchings. Finally, the ability to increase the accuracy of our proposal is confirmed by the evaluation of the application.

6.REFERENCES

1. S. Angizi, Z. He, N. Bagherzadeh, and D. Fan, "Design and evaluation of a spintronic in-memory processing platform for non-volatile data encryption," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., to be published. [Online].
2. Awad, P. Manadhata, S. Haber, Y.Solihin, and W. Horne, "Silent shredder: Zero-cost shredding for secure non-volatile main memory controllers," ACM SIGPLAN Notices, vol. 15, no. 4, pp. 263–276, 2016.
3. E. B. Barker et al., "Guideline for using cryptographic standards in the federal government: Directives, mandates and policies," Tech. Rep. Special Publication (NIST SP)-800-175A, Aug. 2016. [Online]. Available: https://www.nist.gov/publications/guideline-usingcryptographic-standards-federal-government-directives-mandates-and
4. K. Chen, S. Li, N. Muralimanohar, J. H. Ahn, J. B. Brockman, and N. P. Jouppi, "CACTI-3DD: Architecture-level modeling for 3D diestacked DRAM main memory," in Proc. Design, Automat. Test Eur.Conf. Exhib. (DATE), Mar. 2012, pp. 33–38.
5. S. Chhabra and Y. Solihin, "i-NVMM: A secure non-volatile main memory system with incremental encryption," in Proc. 38thAnnu.Int.Symp. Comput. Archit. (ISCA), pp. 177–188, 2011.
6. P. Chown, Advanced Encryption Standard (AES) Ciphersuites for Transport Layer Security (TLS), document RFC 3268, 2002. [Online]. Available: http://www.rfc-editor.org/info/rfc3268
7. P. Colp et al., "Protecting data on smartphones and tablets from memory attacks," in Proc. 20th Int. Conf. Archit. Support Program. Lang. Oper. Syst., 2015, pp. 177–189.
8. X. Dong, C. Xu, Y. Xie, and N. P. Jouppi, "Nvsim: A circuit-level performance, energy, and area model for emerging nonvolatile memory," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 7, no. 31, pp. 994–1007, Jul. 2012.
9. D. Fan, S. Angizi, and Z. He, "In-memory computing with spintronic devices," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), Jul. 2017, pp. 683–688.
10. J. A. Halderman et al., "Lest we remember: Cold-boot attacks on encryption keys," Commun. ACM, vol. 52, no. 5, pp. 91–98, 2009, pp. 45–60.

11. P. Hamalainen, T. Alho, M. Hannikainen, and T. D. Hamalainen, "Design and implementation of low-area and low-power aes encryption hardware core," in Proc. 9th EUROMICRO Conf. Digit. Syst. Design, Aug./Sep. 2006, pp.577–583.

12. A. Hay, K. Strauss, T. Sherwood, G. H. Loh, and D. Burger, "Preventing PCM banks from seizing too much power," in Proc. 44th Annu. IEEE/ACM Int. Symp. Microarchitecture (MICRO), Dec. 2011, pp. 186–195.